

Project Name: PIBTDL/LC AIO
Project Code: 3PD01Z010001
PCB Number : 14060
PCB Size : 150mmx200mm
PCB Name : LC AIO_Intel BT MB

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15	CPU (POWER) (7/11)		46	(Reserved) GPU:PEC Express (1/5)	
16	CPU (POWER CAP1) (8/11)		47	(Reserved) GPU:IFB(IO) (2/5)	
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18	CPU (VSS) (10/11)		49	(Reserved) GPU:GPIO/STRAP (4/5)	
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20	(Reserved) DDR3L-SODIMM1		51	(Reserved) GPU DDR3 128MX16	
21	DDR3L-SODIMM2		52	(Reserved) GPU POWER Sequence	
22	(Reserved) Front BD Connector		53	(Reserved) GPU_CTF/PPLAY/LDO/MVDD	
23	AUDIO CODEC-ALC269Q		54	(Reserved) GPU VDDC_NCP81172	
24	Combo Jack & Speaker		55	PWR DCIN JACK	
25	LAN RTL8111GA		56	PWR_CPU CORE&VNN	
26	RTS5170 (CARD READER)		57	PWR 5V/3D3V	
27	RUN POWER & SEQUENCE		58	PWR 1D8V_S5	
28	(Reserved) Aspire Link		59	PWR 1D35V_OD675_TP851363	
29	LCD CONN/CVR		60	PWR_CPU 1V_S0&CPU 1V_S5	
30	HDMI OUT		61	PWR 1P5_S0&1P05_S0&1P8V_S0	
31	(Reserved) HDMI IN		62	PWR 12V	

KC.BTD01.29C : Bay Trail-D PENTIUM J2900 4C 2.4G C0
KC.BTD01.19C : Bay Trail-D CELERON J1900 4C 2.0G C0
KC.BTD01.18C : Bay Trail-D CELERON J1800 2C 2.4G C0
KC.29301.BMC : Bay Trail-M CELERON N2930 1.86G

071.00BAY.0C6U : Bay Trail-D PENTIUM J2900 4C 2.4G C0
071.00BAY.0C4U : Bay Trail-D CELERON J1900 4C 2.0G C0
071.00BAY.0C5U : Bay Trail-D CELERON J1800 2C 2.4G C0

XTAL Description

XTAL	Function	Frequency	Spec	Capacitance
X1801	CPU	25M	+/-30ppm CL:12P	C1814=12pF C1815=12pF
X1802	CPU	32.768K	+/-20ppm CL:7P	C1817=4pF C1818=4pF
X3	LAN	25M	+/-30ppm CL:12P	C294=15pF C295=15pF
X3501	HUB	12M	+/-20ppm CL:20P	C4603=18pF C4604=18pF
X5	SCALAR	14.318M	+/-20ppm CL:20P	C532=15pF C533=15pF
X7	GPU	27M	+/-30ppm CL:12P	C738=10pF C734=10pF

BOM Configuration

O_ : OCP
O6_ : 65W adaptor
O9_ : 90W adaptor
R_ : Reserve
ECIO_ : ITE8732
SIO_ : ITE8772
L18_ : 18 inch Panel
L19_ : 19.5 inch Panel
CMI_ : CHIMEI Panel
ODT_ : ODT Panel

CPU: INTEL BAY TRAIL-D
J2900 - KC.BTD01.29C
J1900 - KC.BTD01.19C
J1800 - KC.BTD01.18C

SIO: IT8732F
BX - 71.08732.00E
CX - 71.08732.A0E
SCALAR: RTD2486
71.02486.D0G
LAN: RTL8111GA
71.08111.Y03
Audio Codec: ALC269Q
71.00269.H03
Amplifier: TAS5707
74.05707.01T
USB3.0 redriver: PS8713
71.08713.003
SATA3.0 redriver: PS8520
71.08520.003
LVDS translator: RTD2136
71.02136.B04

CMI 19.5"
1.L19_
2.SIO_
3.O_
4.O6_
5.CMI_

ODT 18.5"
1.L18_
2.SIO_
3.O_
4.O6_
5.ODT_

<Variant Name>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichang, Taipei

Title

Cover Page

Size

Document Number

Rev

Customer

Low Cost AIO

1A

Date:

Friday, September 12, 2014

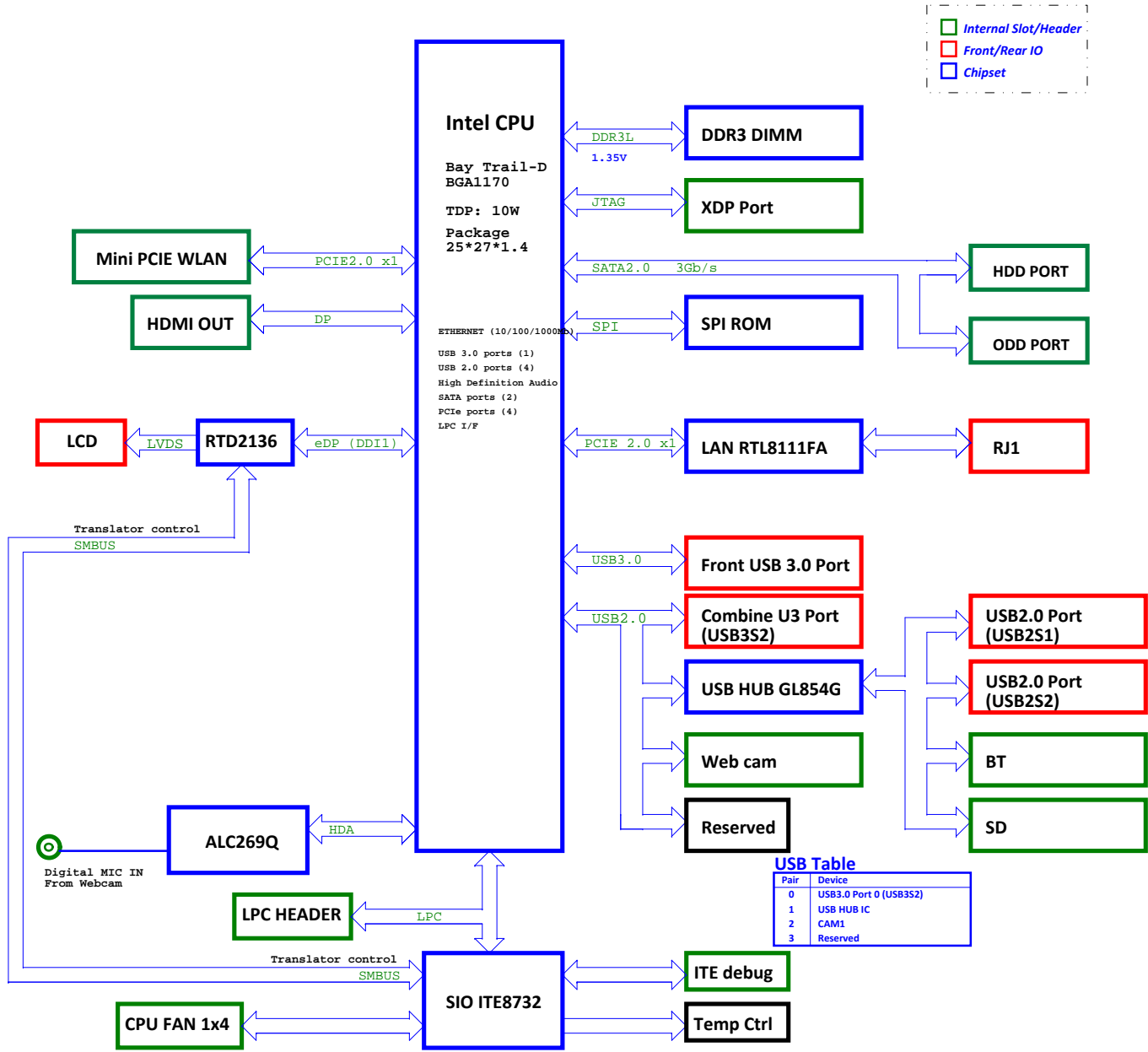
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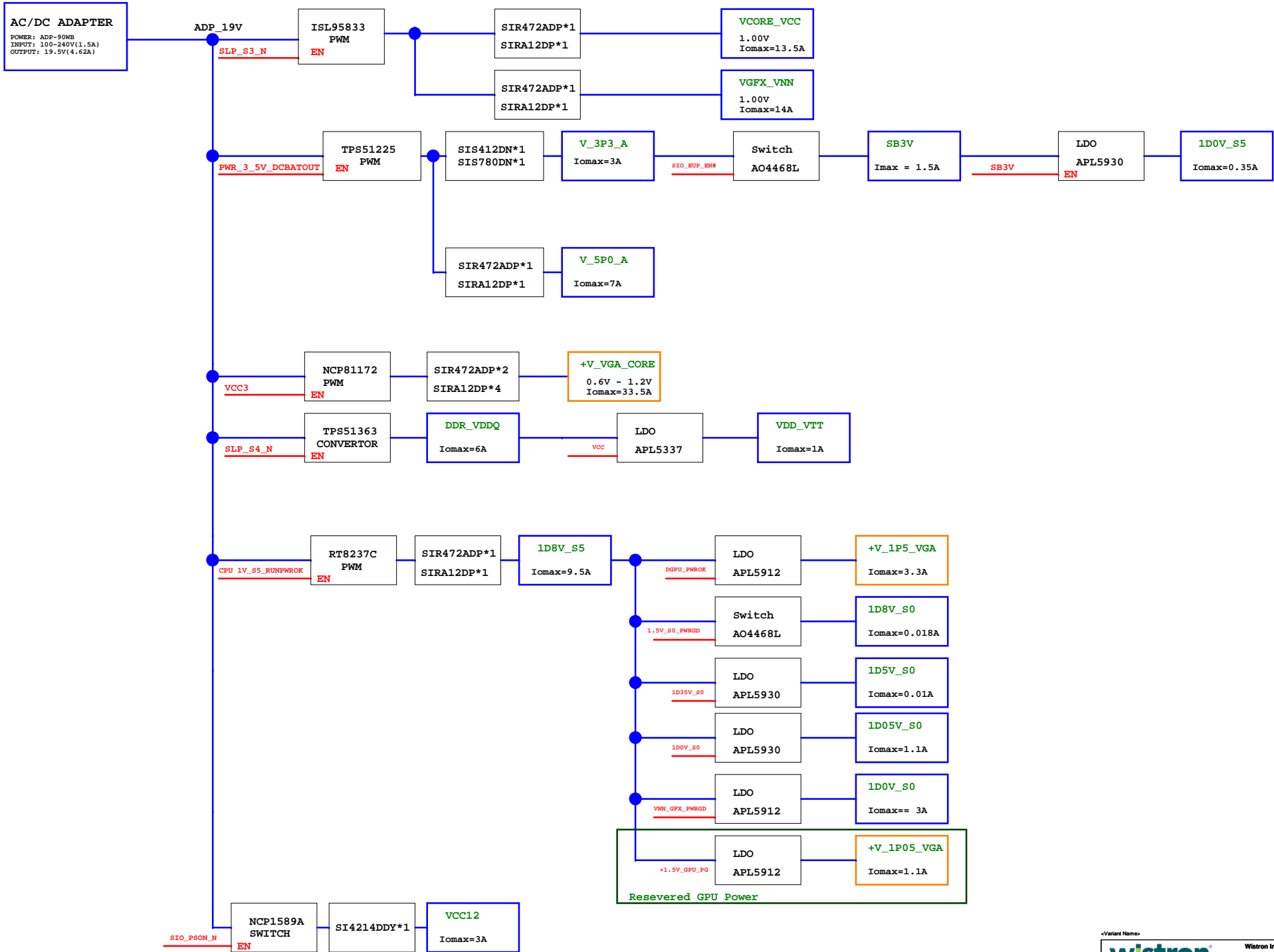
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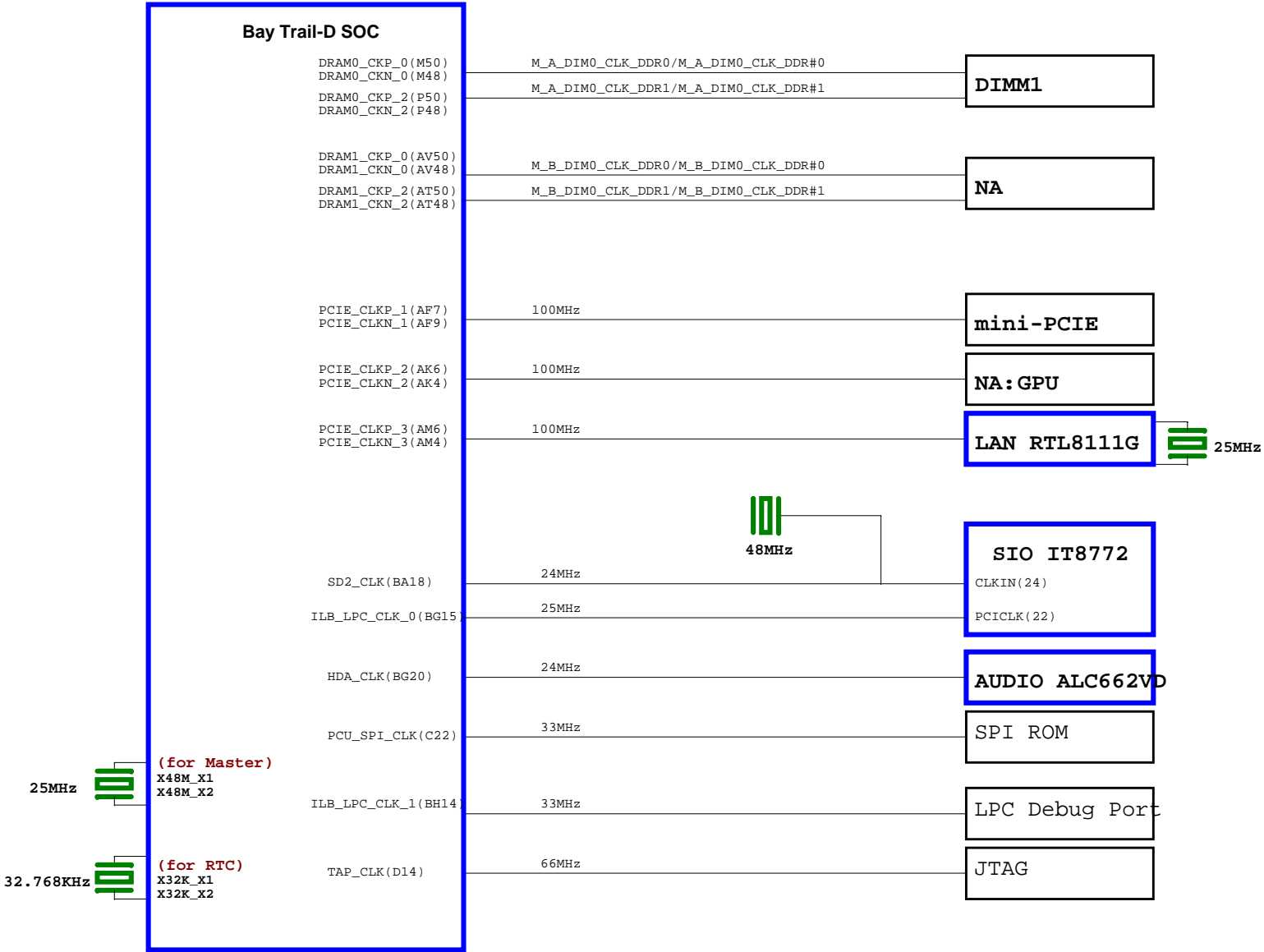
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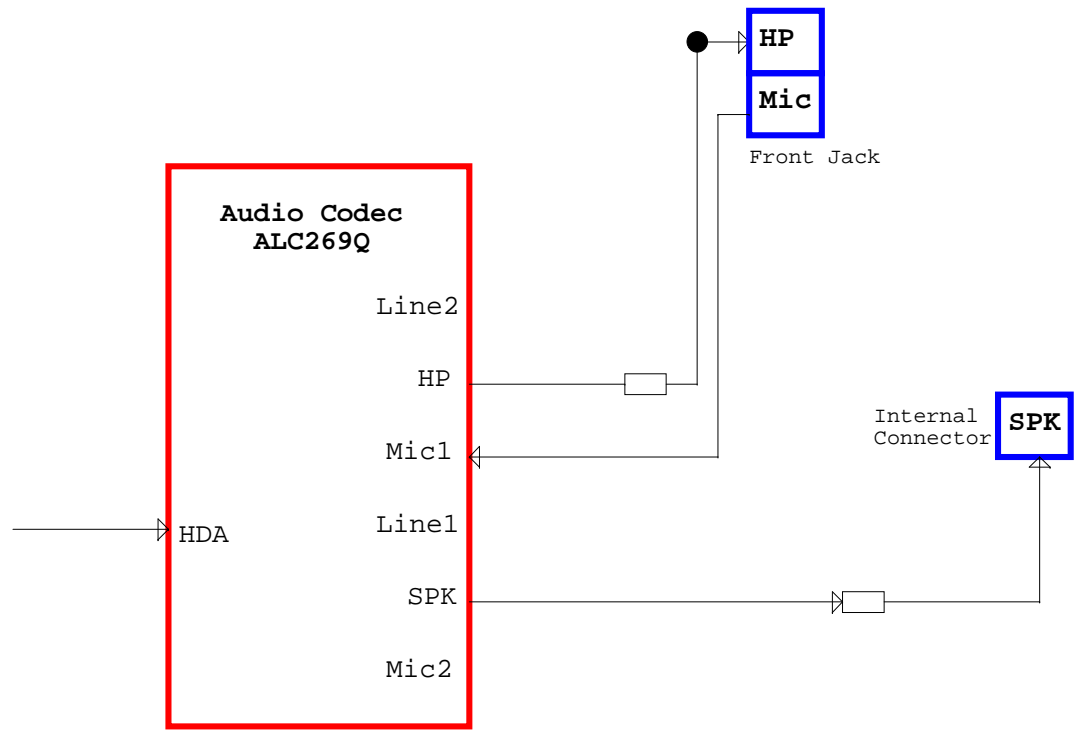


USB Table

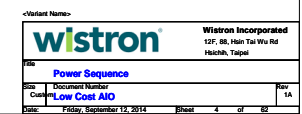
Pair	Device
0	USB3.0 Port 0 (USB3S2)
1	USB HUB IC
2	CAM1
3	Reserved







Source	Destination	Signal
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Dallas GPIO Table

Version: 2012/11/27

IC Pin Name	Power Well	Default	Default State	Signal Name	Usage	BMOS Programming					Comment
						S0	S1	S3	S4	S5	
GENINT1_L/GPIO32	VDD_33	null	Input, 15K PU	no use	no use						
GENINT2_L/GPIO33	VDD_33	null	Input, 15K PU	no use	no use						
SCLO/GPIO43	VDD_33	null	Input	SMBUS_CLK	SMBUS0	Native	Native	Native	Native	Native	2.2K to 3D3V_S0
SD_LED/GPIO45	VDD_33	null	Output	no use	no use						
SDAQ/GPIO47	VDD_33	null	Input	SMBUS_DATA	SMBUS0	Native	Native	Native	Native	Native	2.2K to 3D3V_S0
SERIRQ/GPIO48	VDD_33	SERIRQ	Input, 15K PU	SERIRQ_N	SERIRQ	Native	Native	Native	Native	Native	10k(R) to 3D3V_S0
GPIO49	VDD_33	GPIO49	Input	no use	no use						
GPIO50	VDD_33	GPIO50	Input, 15K PU	KEY0_TEST	BTN test	GPI	GPI	GPI	GPI	GPI	1K to 3D3V_S0
GPIO51	VDD_33	GPIO51	Input	TP51	no use						
FANOUT0/GPIO52	VDD_33	null	Output, 15K PU	no use	no use						
DEVSLP[0]/GPIO55	VDD_33	GPIO55	Input, 15K PU	TP29	no use						
FANIN0/GPIO56	VDD_33	null	Input, 15K PU	no use	no use						
GPIO57	VDD_33	GPIO57	Input, 15K PU	TP48	no use						
GPIO58	VDD_33	GPIO58	Input, 15K PU	TP49	no use						
DEVSLP[1]/GPIO59	VDD_33	GPIO59	Input, 15K PU	PANEL_OFF_R	panel ON/OFF	GPI	GPI	GPI	GPI	GPI	EC: 10k to 3D3V_A scalar: 10k to P3P3V
CLK_REQ0_L/ SATA_I0_L/ SATA_ZP0_L/GPIO60	VDD_33	null	Input, 15K PU	BLANCLK_REQ_N_1	clock request (Reserved)						10k(R) to 3D3V_S0
CLK_REQ1_L/GPIO61	VDD_33	null	Input, 15K PU	CLK_PCIE_WLAN_REQ#	clock request (Reserved)						
CLK_REQ2_L/GPIO62	VDD_33	null	Input, 15K PU	no use	no use						
CLK_REQ3_L/ SATA_IS1_L/ SATA_ZP1_L/GPIO63	VDD_33	null	Input, 15K PU	no use	no use						
GPIO64	VDD_33	GPIO64	Input, 15K PU	SMBUS_SSP	scalar FW	GPO L	GPO L	GPO L	GPO L	GPO L	100k to GND controlled by SW tool
CLK_REQ0_L/GPIO65/ OSCIN	VDD_33	null	Input, 15K PU	PEG_CLKREQ#	clock request (Reserved)						
SPKR/GPIO66	VDD_33	SPKR	Output	SPKR	beep	Native	Native	Native	Native	Native	
SATA_ACT_L/GPIO67	VDD_33	SATA_ACT_L	Output	no use	no use						
GPIO68	VDD_33	GPIO68	Input, 15K PU	SYS_ID2	SYS ID	GPI	GPI	GPI	GPI	GPI	
GPIO69	VDD_33	GPIO69	Input, 15K PU	SYS_ID3	SYS ID	GPI	GPI	GPI	GPI	GPI	
GPIO70	VDD_33	GPIO70	Input, 15K PU	APU_PROCHOT#_R	thermal (Reserved)						1K to 3D3V_S0
GPIO71	VDD_33	GPIO71	Input	SYS_ID1	SYS ID	GPI	GPI	GPI	GPI	GPI	
SD_CLK/SCUK_2/ GPIO73	VDD_33	null	Input, 50K PU	no use	no use						
SD_CMD/GPIO74	VDD_33	null	Input, 50K PU	no use	no use						
SD_CD/GPIO75	VDD_33	null	Input, 50K PU	no use	no use						
SD_WP/GPIO76	VDD_33	null	Input, 50K PU	no use	no use						
SD_DATA0/SDAT1_2/ GPIO77	VDD_33	null	Input, 50K PU	no use	no use						
SD_DATA1/SDAT0_2/ GPIO78	VDD_33	null	Input, 50K PU	no use	no use						
SD_DATA2/GPIO79	VDD_33	null	Input, 50K PU	no use	no use						
SD_DATA3/GPIO80	VDD_33	null	Input, 50K PU	no use	no use						
SPI_WP_L/GPIO161	VDD_33_ALW	SPI_WP_L	Input	ROM_RST#	SPI	Native	Native	Native	Native	Native	10k to 3D3V_S5
SPI_CLK/GPIO162	VDD_33	SPI_CLK	Input, 15K PD	SPI_CLK	SPI	Native	Native	Native	Native	Native	
SPI_DO/GPIO163	VDD_33_ALW	SPI_DO	Input, 15K PD	SPI_DATAOUT	SPI	Native	Native	Native	Native	Native	
SPI_DI/GPIO164	VDD_33_ALW	SPI_DI	Input, 15K PD	SPI_DATAIN	SPI	Native	Native	Native	Native	Native	
SPI_CS1_L/GPIO165	VDD_33	SPI_CS1_L	Input, 15K PU	SPI_CS0_N	SPI	Native	Native	Native	Native	Native	10k to 3D3V_S5
SPI_CS2_L/GPIO166	VDD_33	SPI_CS2_L	Input, 15K PU	EDID_RDY	EDID for APU	GPI	GPI	GPI	GPI	GPI	10k to 3D3V_S5
AZ_S0IN0/GPIO167	VDD_33_ALW	AZ	Input, 13.6K PD	AZ_S0IN0	AZ	Native	Native	Native	Native	Native	10k(R) to GND
AZ_S0IN1/GPIO168	VDD_33_ALW	AZ	Input, 13.6K PD	AZ_S0IN1	AZ	Native	Native	Native	Native	Native	10k(R) to GND
AZ_S0IN2/GPIO169	VDD_33_ALW	AZ	Input, 13.6K PD	AZ_S0IN2	AZ	Native	Native	Native	Native	Native	10k(R) to GND
AZ_S0IN3/GPIO170	VDD_33_ALW	AZ	Input, 13.6K PD	AZ_S0IN3	AZ	Native	Native	Native	Native	Native	10k(R) to GND
GPIO174	VDD_33_ALW	GPIO 174	Input	Wake#_PCIE	wake up	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 3D3V_S5
IR_LED_L/LB_L/GPIO184	VDD_33_ALW	null	Input, 15K PU	Wake#_LOM	wake up	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 3D3V_S5
SC11/GPIO227	VDD_33_ALW	null	Input	SMB1_CLK	SMBUS1	Native	Native	Native	Native	Native	2.2K to 3D3V_S5
SDA1/GPIO228	VDD_33_ALW	null	Input	SMB1_DATA	SMBUS1	Native	Native	Native	Native	Native	2.2K to 3D3V_S5
GA20IN/GEVENT0#	VDD_33	GA20 IN	Input, 15K PU	KA20GATE	GA20IN	Native	Native	Native	Native	Native	10k(R) to 3D3V_S0
GEVENT2#	VDD_33_ALW	null	Input, 15K PU	SPI_SW	only strapping						strap low
LPC_PME#/ GEVENT3#	VDD_33_ALW	null	Input, 15K PU	PME#_M	LPC	Native	Native	Native	Native	Native	2.2k(R) to 3D3V_S5
GEVENT4#	VDD_33_ALW	null	Input	THERMAL_SHUT#	thermal (Reserved)						10k(R) to 3D3V_S5
LPC_PDR/ GEVENT5#	VDD_33_ALW	null	Output	TP_LPC_PDR#	no use						
IR_TX1/ GEVENT6#	VDD_33_ALW	null	Input, 15K PU	no use	no use						
GEVENT7#	VDD_33_ALW	null	Input	EC_SMI#	(Reserved)						10k to 3D3V_S5
WAKE#/ GEVENT8#	VDD_33_ALW	null	Input, 15K PU	PCIE_WAKE#	wake up	Native	Native	Native	Native	Native	10k to 3D3V_S5
SPI_HOLD#/ GEVENT9#	VDD_33_ALW	Strap	Input	SST_HOLD#_1_R	SPI	Native	Native	Native	Native	Native	10k to 3D3V_S5
GEVENT10#	VDD_33_ALW	null	Input, 15K PU	no use	no use						
GEVENT11#	VDD_33_ALW	null	Input, 15K PU	no use	no use						
USB_OC0#/SPI_TPM_CS#/ TRST#/ GEVENT12#	VDD_33_ALW	USB_OC0#	Input, 15K PU	USB_OC_01	USB OCP	Native	Native	Native	Native	Native	10k to 3D3V_S5
USB_OCI#/TDI/ GEVENT13#	VDD_33_ALW	null	Input, 15K PU	USB_OC_23	USB OCP	Native	Native	Native	Native	Native	10k to 3D3V_S5
USB_OC2#/TCK/ GEVENT14#	VDD_33_ALW	null	Input, 15K PU	no use	no use						
USB_OC3#/TDO/ GEVENT15#	VDD_33_ALW	null	Input, 15K PU	no use	no use						
AC_PRES#/IR_RX0/ GEVENT16#	VDD_33_ALW	null	Input, 15K PU	AC_PRES	no use						
GEVENT17#	VDD_33_ALW	null	Input, 15K PU	no use	no use						
BLINK/ GEVENT18#	VDD_33_ALW	null	Input, 15K PU	no use	no use						
SYS_RESET#/ GEVENT19#	VDD_33_ALW	SYS_RESET_L	Input, 15K PU	FP_RST_N	no use						
IR_RX1/ GEVENT20#	VDD_33_ALW	null	Input, 15K PU	no use	no use						
IR_TX0/ GEVENT21#	VDD_33_ALW	null	Input, 15K PU	no use	no use						
GEVENT22#	VDD_33_ALW	null	Input, 15K PU	no use	no use						
LPC_SMI#/ GEVENT23#	VDD_33_ALW	null	Input, 15K PU	no use	no use						

IC Pin Name	Power Well (GPIO)	Default	Default State	Signal Name	Usage	Open Drain / Push Pull	BIOS Programming					Comment
							S0	S1	S3	S4	S5	
PCIRST3#/GP10	3V5B	PCIRST3#	Native	AMP_PDN#	mute	DO/DI/O	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 3D3V_A controlled by EC H: ON, L: OFF/mute
PCIRST2#/GP11	3V5B	PCIRST2#	Native	PCIRST2#	RESET	DO/DI/O	Native	Native	Native	Native	Native	10k(R) to 3D3V_A
PCIRST1#/GP12	3V5B	PCIRST1#	Native	PCIRST1#	RESET	DO/DI/O	Native	Native	Native	Native	Native	10k(R) to 3D3V_A
PWROK1/GP13	3V5B	PWROK1	Native	PWROK3_1	PWROK	DOD/DI/O	Native	Native	Native	Native	Native	1k to 3D3V_S0 set delay to 200ms
VCORE_EN/PCN_C1/GP14	3V5B	VCORE_EN	Native	LAN_PWR_EN	LAN power (reserved)	DOD/DI/O/DI/O	GPO H	GPO H	GPO H	GPO H	GPO H	390k to 3D3V_S5
PCIRST1#N/CIRTX2/GP15/CPU_PG	3V5B	CIRTX2	Native	SIO_PCIRST1#N	RESET	DI/DOD/DI/O/DOD	Native	Native	Native	Native	Native	10k to 3D3V_A
SVS8_CTRL#/ CIRRX2/GP16	3V5B	SVS8_CTRL#	Native	EC_EUP	EUP	DOD/DI/DI/O	Native	Native	Native	Native	Native	10k to 3D3V_A
RI2H/GP17	3V5B	null		SPI_WP_R_N	SPI WP	DI/DI/O	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 3D3V_A H: can write L: write protect
CTS2H/GP20	3V5B	GP20		PANEL_SW_EC	panel ON/OFF	DI/DI/O	GPI	GPI	GPI	GPI	GPI	10k to 3D3V_A controlled by EC
DCD2H/GP21	3V5B	GP21		PANEL_CTRL	panel ctrl (reserved)	DI/DI/O	GPI	GPI	GPI	GPI	GPI	10k to 3D3V_A controlled by EC
SKC/GP22	3V5B	GP22		SIO_SCK_R	EC EPROM	DO/DI/O	Native	Native	Native	Native	Native	1k to 3D3V_A
SI/GP23	3V5B	GP23		SIO_SI	EC EPROM	DO/DI/O	Native	Native	Native	Native	Native	1k to 3D3V_A
RTS2H/GP24	3V5B	GP24		THERMAL_SHUT#_SIO	thermal (reserved)	DO/DI/O	GPO H	GPO H	GPO H	GPO H	GPO H	10k(R) to 3D3V_S5
DSR2H/GP25	3V5B	GP25		SIO_Audio_Mute	mute (reserved)	DI/DI/O	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 3D3V_A
SOULT2/GP26	3V5B	GP26		SIO_UART1_TX	UART	DO/DI/O	Native	Native	Native	Native	Native	10k to 3D3V_A
SIN2/GP27	3V5B	GP27		SIO_UART1_RX	UART	DI/DI/O	Native	Native	Native	Native	Native	10k to 3D3V_A
ATXPG/GP30	3V5B	ATXPG	Native	SIO_ATXPG	sequence	DI/DI/O	Native	Native	Native	Native	Native	10k to 3D3V_S0
PWMOUT/GP31	3V5B	PWMOUT	Native	W3_DISABLE_N	wake up	DOD/DI/O	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 3D3V_S5 L: disable
DPWROK/GP32	3V5B	DPWROK	Native	W1_DISABLE_N	wake up	DOD/DI/O	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 3D3V_S5 L: disable
SUSACK#/GP33	3V5B	SUSACK#	Native	SIO_BOARD_ID3	board ID	DOD/DI/O	GPI	GPI	GPI	GPI	GPI	controlled by EC H: scalar, L: non-scalar
SUSWARN#/GP34	3V5B	SUSWARN#	Native	SIO_BOARD_ID2	board ID	DOD/DI/O	GPI	GPI	GPI	GPI	GPI	board stage
FAN_TAC4/GP35	3V5B	FAN_TAC4	Native	SIO_BOARD_ID1	board ID	DI/DI/O	GPI	GPI	GPI	GPI	GPI	board stage
FAN_CTL3/GP36	3V5B	FAN_CTL3	Native	no use	no use	DOD/DI/O	GPO H	GPO H	GPO H	GPO H	GPO H	
FAN_TAC3/GP37	3V5B	FAN_TAC3	Native	EC_AMP_RST	mute	DI/DI/O	GPO L	GPO L	GPO L	GPO H	GPO H	10k to 3D3V_A controlled by EC H: reset/mute, L: normal
SVSBSW#/GP40	3V5B	SVSBSW#	Native	SLP_S3_N_R3	sequence	DOD/DI/O	GPI	GPI	GPI	GPI	GPI	10k to 3D3V_S5 controlled by EC
PWROK2/GP41	3V5B	PWROK2	Native	PWROK3_2	PWROK (reserved) S0 power (reserved)	DOD/DI/O	Native	Native	Native	Native	Native	10k to 3D3V_S5
PSON#/GP42	3V5B	PSON#	Native	SIO_PSON_N		DOD/DI/O	Native	Native	Native	Native	Native	4.7k to 3D3V_A
PANSWH#/GP43	3V5B	PANSWH#	Native	PB_IN_N_1	PWR BTN	DI/DI/O	Native	Native	Native	Native	Native	330k to 3D3V_A
PWRONH#/GP44	3V5B	PWRONH#	Native	SW_ON_N_SIO	sequence	DOD/DI/O	Native	Native	Native	Native	Native	10k to 3D3V_S5
D_RX0/SMCLK2_/ GP46	3V5B	null		SMBCLK2_SIO	SIO SMBUS2	DI/DIO/DI/O	Native	Native	Native	Native	Native	10k to 3D3V_A controlled by EC
D_TX0/SDMAT2_/ GP47	3V5B	null		SMBDAT2_SIO	SIO SMBUS2	DO/DIO/DI/O	Native	Native	Native	Native	Native	10k to 3D3V_A controlled by EC
SO/GP50	3V5B	S0	Native	SIO_S0	EC EPROM	DI/DI/O	Native	Native	Native	Native	Native	1k to 3D3V_A
FAN_CTL2/GP51	3V5B	FAN_CTL2	Native	SUSLED_R_N	LED	DOD/DI/O	Native	Native	Native	Native	Native	10k to USB90_VCCA
FAN_TAC2/GP52	3V5B	FAN_TAC2	Native	EC_SMI#	(Reserved)	DI/DI/O	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 3D3V_S5
SUSCB#/GP53	3V5B	SUSCB#	Native	SLP_S5_N_R	sequence	DI/DI/O	Native	Native	Native	Native	Native	10k to 3D3V_S5
PME#/GP54	3V5B	PME#	Native	LPC_PME_N	LPC	DOD/DI/O	Native	Native	Native	Native	Native	2.2k(R) to 3D3V_S5
RSMRST#/CIRRX1/GP55	3V5B	RSMRST#	Native	ICH_RSMRST_N_R	sequence	DOD/DI/DI/O	Native	Native	Native	Native	Native	10k to 3D3V_S5
MCLK/GP56	3V5B	MCLK	Native	MCLK	no use	DIOD/DI/O	Native	Native	Native	Native	Native	10k to SV_S5
MDAT/GP57	3V5B	MDAT	Native	MDAT	no use	DIOD/DI/O	Native	Native	Native	Native	Native	10k to SV_S5
KCLK/GP60	3V5B	KCLK	Native	KBCLK	no use	DIOD/DI/O	Native	Native	Native	Native	Native	10k to SV_S5
KDAT/GP61	3V5B	KDAT	Native	KDAT	no use	DIOD/DI/O	Native	Native	Native	Native	Native	10k to SV_S5
KRST#/GP62	3V5B	KRST#	Native	KBRST_N	KBRST	DO/DI/O	Native	Native	Native	Native	Native	10k(R) to 3D3V_S0
SLP_SUS#/VLDT_EN/GP63	3V5B	SLP_SUS#	Native	APU_PROCHOT#	(Reserved)	DI/DO/DI/O	GPI	GPI	GPI	GPI	GPI	1k to 3D3V_S0 controlled by EC
GP70/KSIO	3V5B	KSIO	Native	DET_HDMI	scalar/HDMI	DI/O/DI	GPI	GPI	GPI	GPI	GPI	10k to 3D3V_A controlled by EC
GP71/KS11	3V5B	KS11	Native	SCALAR_EN	scalar/HDMI	DI/O/DI	GPO H	GPO H	GPO H	GPO L	GPO L	10k to 3D3V_A controlled by EC H: enable scalar
GP72/KS00	3V5B	KS00	Native	EUP_DSW_SEL	strap	DI/O/DI/O	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 3D3V_A
GP73/KS01	3V5B	KS01	Native	SIO_PANEL_ON	panel ON/OFF	DI/O/DI/O	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 3D3V_A controlled by EC L: panel ON
GP74/KS02	3V5B	KS02	Native	SIO_PANEL_OFF	panel ON/OFF	DI/O/DI/O	GPO H	GPO H	GPO H	GPO H	GPO H	10k to 3D3V_A controlled by EC L: panel OFF
GP75/KS03	3V5B	KS03	Native	LVDS_BL_EN_1	panel ON/OFF	DI/O/DI/O	GPI	GPI	GPI	GPI	GPI	10k to 3D3V_A controlled by EC
GP76/KS04	3V5B	KS04	Native	no use	no use	DI/O/DI/O	GPO H	GPO H	GPO H	GPO H	GPO H	
GP77/KS05	3V5B	KS05	Native	SIO_MEM_EVENT_L	power consum. (reserved)	DI/O/DI/O	GPO H	GPO H	GPO H	GPO H	GPO H	controlled by EC
IO_SCiH/GP85/SDMAT0	3V5B			SIO_SDMAT0	SIO SMBUS0	DO/DI/O/DI/O	Native	Native	Native	Native	Native	4.7k to 3D3V_S0 controlled by EC
GP86/SMCLK0	3V5B			SIO_SMCLK0	SIO SMBUS0	DI/O/DI/O	Native	Native	Native	Native	Native	4.7k to 3D3V_S0 controlled by EC

QVL1: Hynix (KN.2GB0G.038)+R221, R220, R231, R238 (64.10025.6DL)
QVL2: Micron (KN.2GB04.022)+R234, R238, R228, R219 (64.10025.6DL)

CHANNEL A:1GB DDR3

KN.2GB0G.038	2Gb	DDR3	128M*16	900MHz	SDRAM	FBGA96P	Hynix	-	H5TC2G63FFR-11C
KN.2GB04.022	2Gb	DDR3	128M*16	900MHz	SDRAM	FBGA96P	Micron	-	MT41J128M16JT-093G:K

VRAM Type	P/N
Hynix 1G H5TC2G63FFR-11C	KN.2GB0G.038
VRAM Type	P/N
Micron 1G MT41J128M16JT-093G:K	KN.2GB04.022

FBCLK Termination place on VRAM side

128M*16 VRAM
KN.2GB0B.040 - Samsung K4W2G1646Q-BC1A
KN.2GB0G.038 - Hynix H5TC2G63FFR-11C

ORDERING INFORMATION

Part No.	Power Supply	Clock Frequency	Data Rate	Interface	Package
H5TC2G63FFR-11C	VDD/VDDQ=1.35V	900MHz	1.8Gbps/pin	SSTL-15	96ball FBGA
	VDD/VDDQ=1.5V	1.0Ghz	2.0Gbps/pin		
H5TC2G63FFR-N1C	VDD/VDDQ=1.5V	1.1Ghz	2.2Gbps/pin		

Note) 1.35v speed part provides backward compatibility with the 1.5V DDR3.

RMA_CFG [3:0]
Samsung - K4W2G1646E-BC11 (1000MHz) [0101]
Micron - MT41J128M16JT-093G:K (1000MHz) [0001]

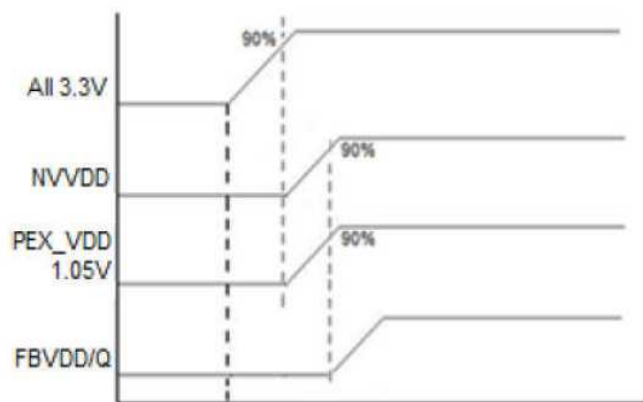
1. Ordering Information

[Table 1] Samsung 2Gb gDDR3 Q-die ordering information table

Organization	gDDR3-1600(11-11-11)	gDDR3-1800(13-13-13) ²	gDDR3L-1800(13-13-13) ²	gDDR3-2133(14-14-14) ²	Package
VDD	1.5V	1.5V	1.35V	1.5V	
128Mx16	K4V2G1646Q-BC12	K4V2G1646Q-BC11		K4V2G1646Q-BC1A	96 FBGA

NOTE
1. Speed bin is in order of CL,RC,CD,RRP.
2. Backward Compatible to gDDR3-1800(13-13-13), gDDR3L-1800(13-13-13)
3. Backward Compatible to gDDR3-1800(13-13-13)

3.3V-->NVVDD&PEX_VDD(+V_VGA_CORE&+V_1P05_VGA)-->FBVDD/Q(+V_1P5_VGA)



Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

<Core Design>

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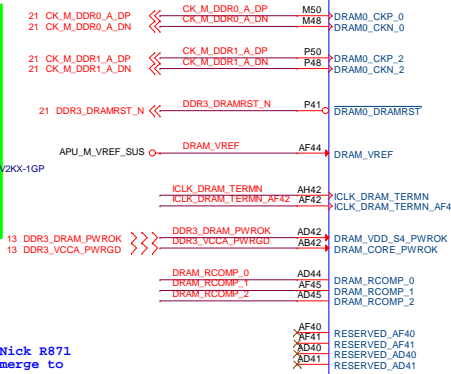
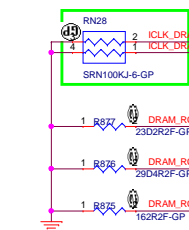
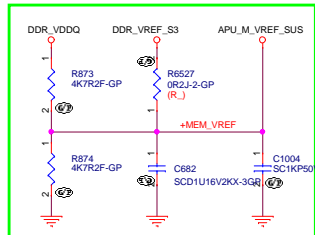
Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
GPU_POWER Sequence

Size B Document Number
Low Cost AIO

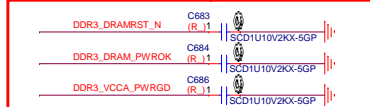
Rev
1A

Date: Friday, September 12, 2014 Sheet 52 of 62



20140509 Nick R871
and R872 merge to
SRN100K

reserve the 0402 0.1u caps on reset for EMI.



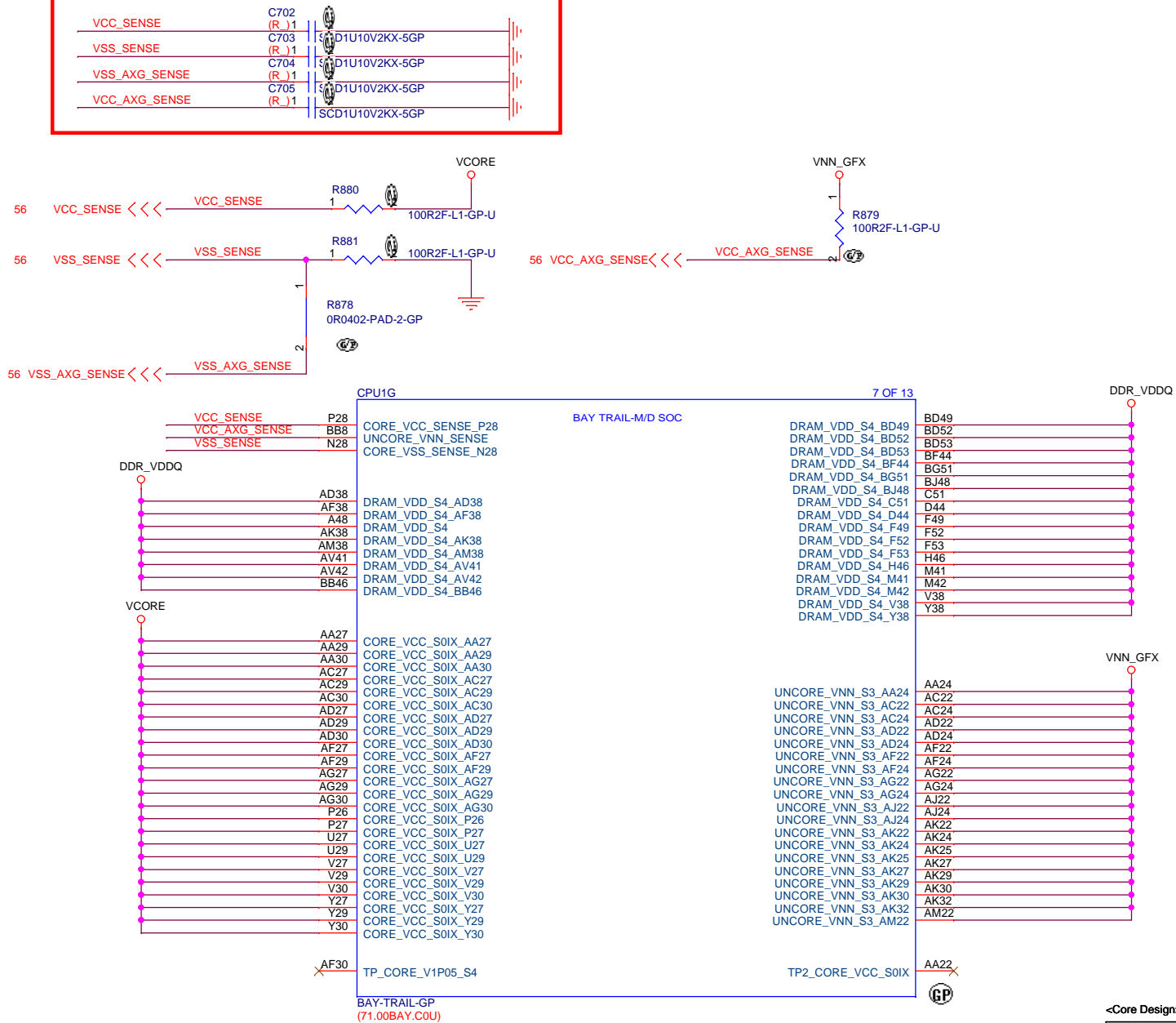
«Core Design»

wistron

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Hsinchu, Taipei

File	CPU (DDR)		
Size	Document Number	Rev	1A
Customer	Low Cost AIO		
Date	Friday, September 12, 2014	Sheet	9 of 62

reserve the 0402 0.1u caps on reset for EMI



<Core Design>

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Hsichih, Taipei

Title

CPU (VCC CORE)

Size

Document Number

Custom

Low Cost AIO

Rev

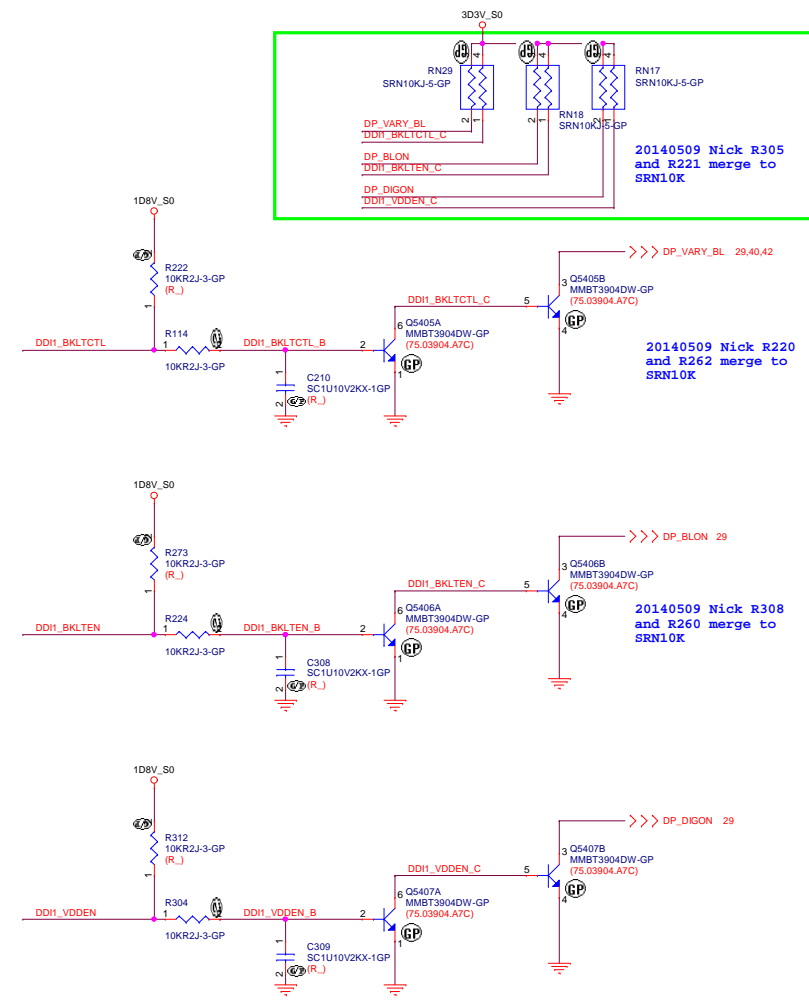
1A

Date:

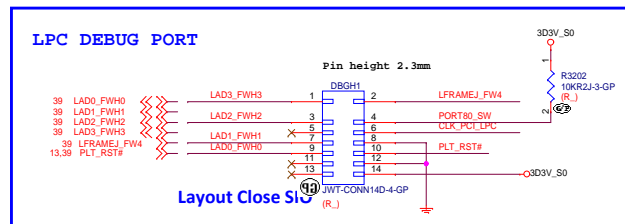
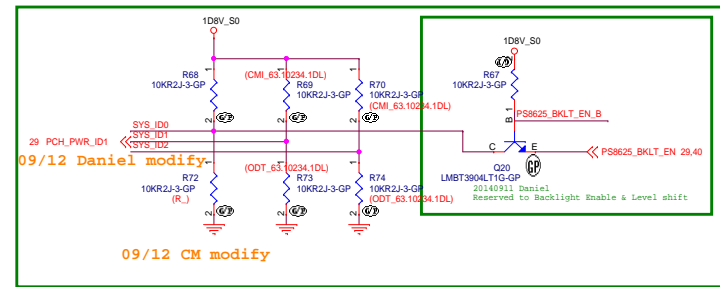
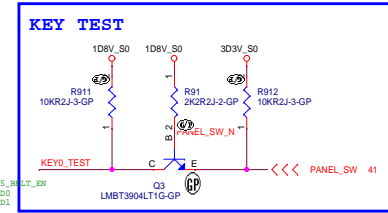
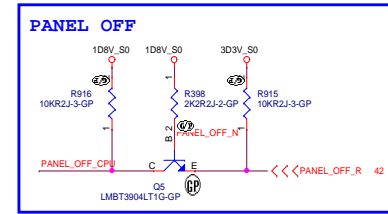
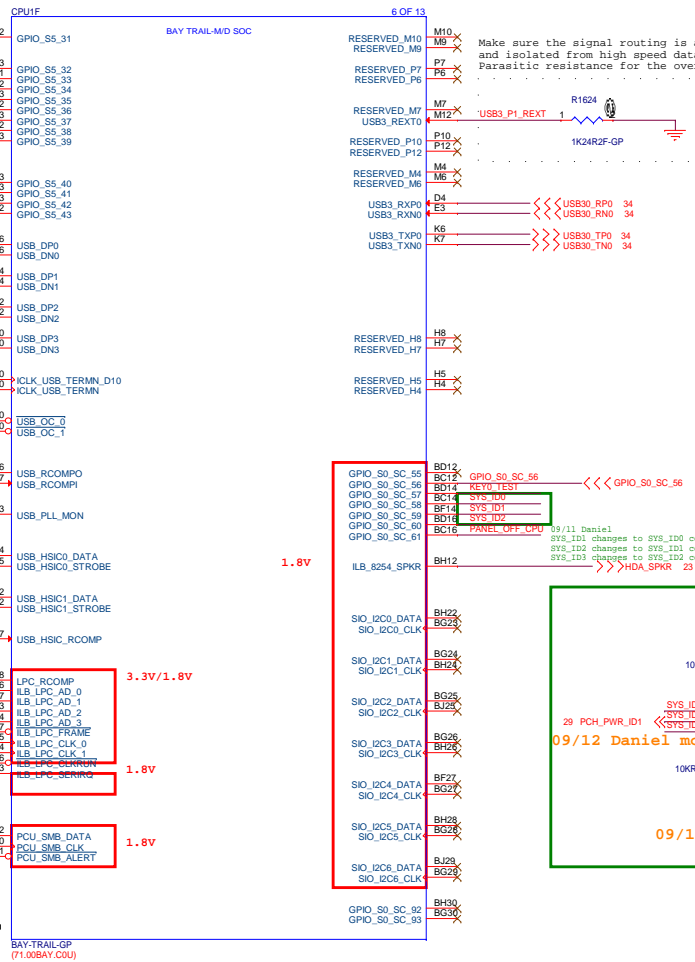
Friday, September 12, 2014

Sheet

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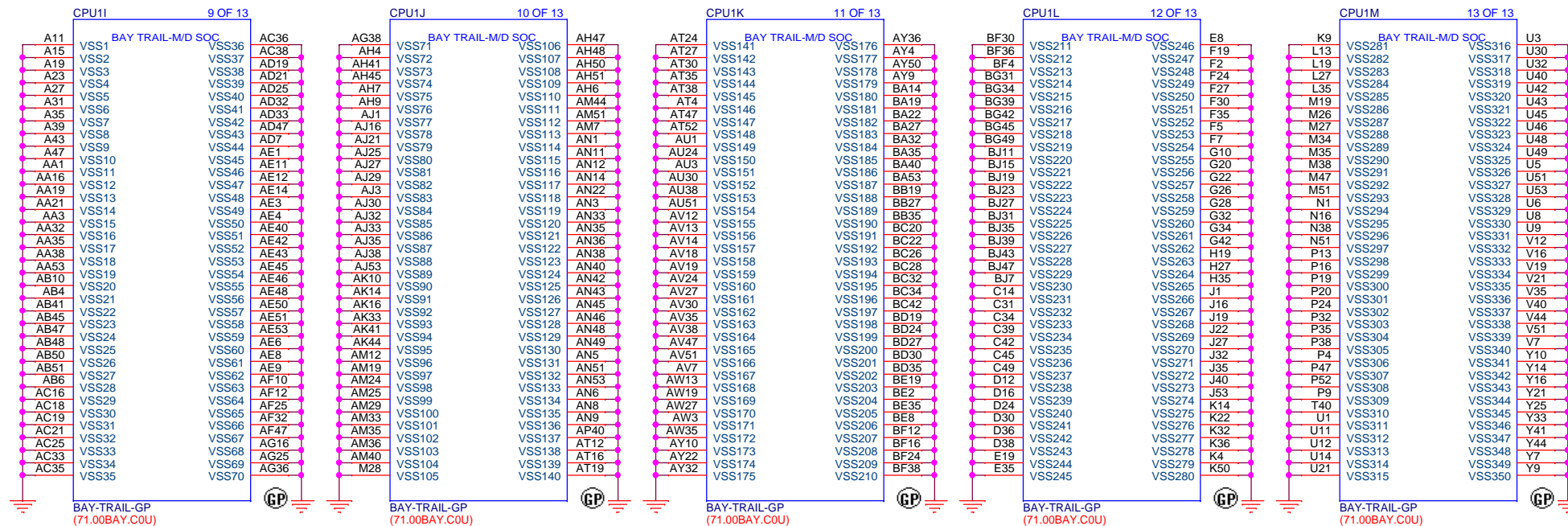


Pair	Device
0	USB3.0 Port 0 (USB3S2)
1	USB HUB IC
2	CAM1
3	Delete TOUCH1



PANEL_BTN_EVENT#_CPU << PANEL_BTN_EVENT# 30



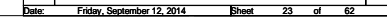


<Core Design>



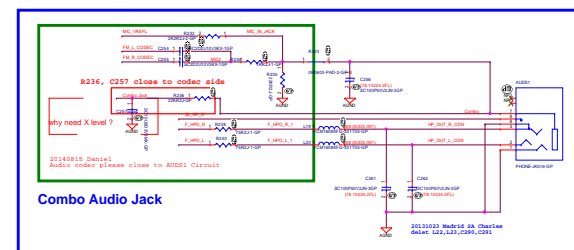
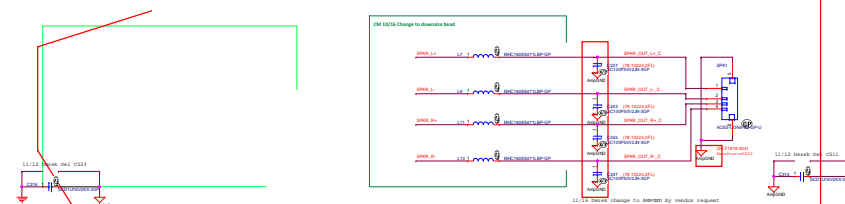
Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title				Rev 1A
CPU (VSS)				
Size	Document Number			Rev 1A
Custom	Low Cost AIO			
Date:	Friday, September 12, 2014	Sheet	18 of 62	



Support iPhone ~ Mount R3018,R3020
unMount R3019,R3021

Support Nokia ~ Mount R3019,R3021
unMount R3018,R3020



SHEN_MUTE_AP_CTL
When the PC mode and Monitor mode are being switched

MUTE_AP_CTL should be low in order to avoid the noise

MUTE_AP_CTL also control wh select MUTE in the PC mode Monitor mode

MUTE_AP_CTL also control wh system wake from S3 to S0



```
Control
23 _IO_M_P_R >>>

Enable Control
Low: Mute
High: SG-MUTE

23 FMI_L_CODEC <<<
23 FMI_R_CODEC <<<
23 SMC_VREFL <<<
23 S_FIO_P_R <<<
23 S_FIO_N_A <<<
14,23,39 AZ_RST_N <<<

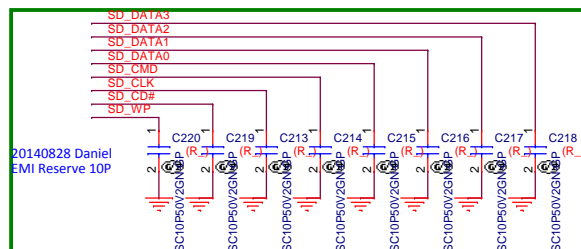
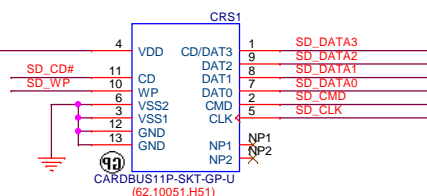
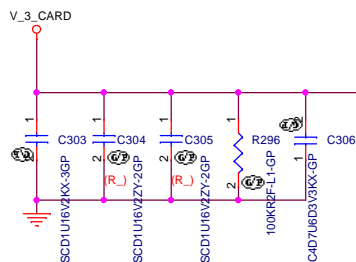
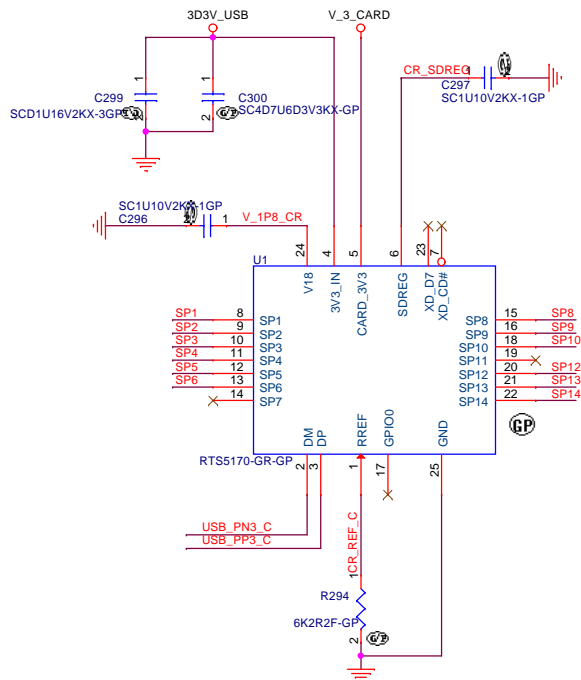
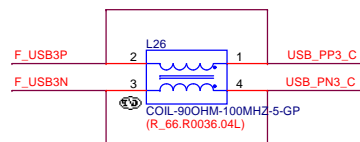
23 SPWR_L+ <<<
23 SPWR_L- <<<
23 SPWR_R+ <<<
23 SPWR_R- <<<

23 Control Jack

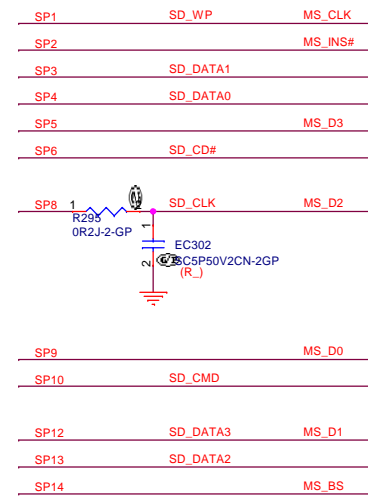
2012/08/28_2Pin_5a
```


(SD only)

35 F_USB3P
35 F_USB3N



3IN1 (MS/SD/MMC) Combo Net



Without card	CD	WP	GND
Inserted card(lock)	CD	WP	GND
Inserted card(unlock)	CD	WP	GND

20140828 Daniel
EMI Reserve 10P

Core-Designs

wistron

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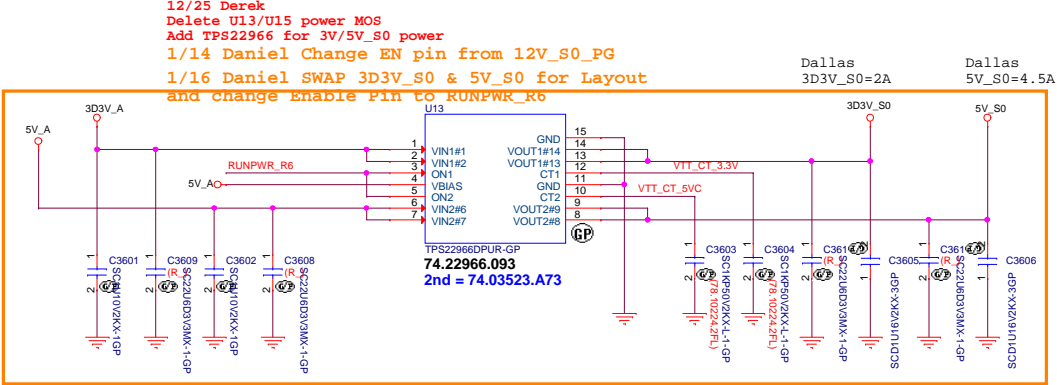
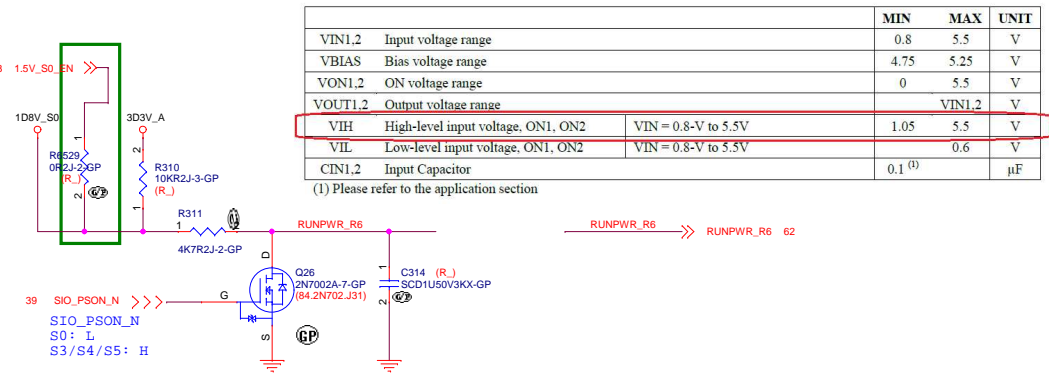
Title
RTS5170 (CARD READER)

Size
Custom Low Cost A10

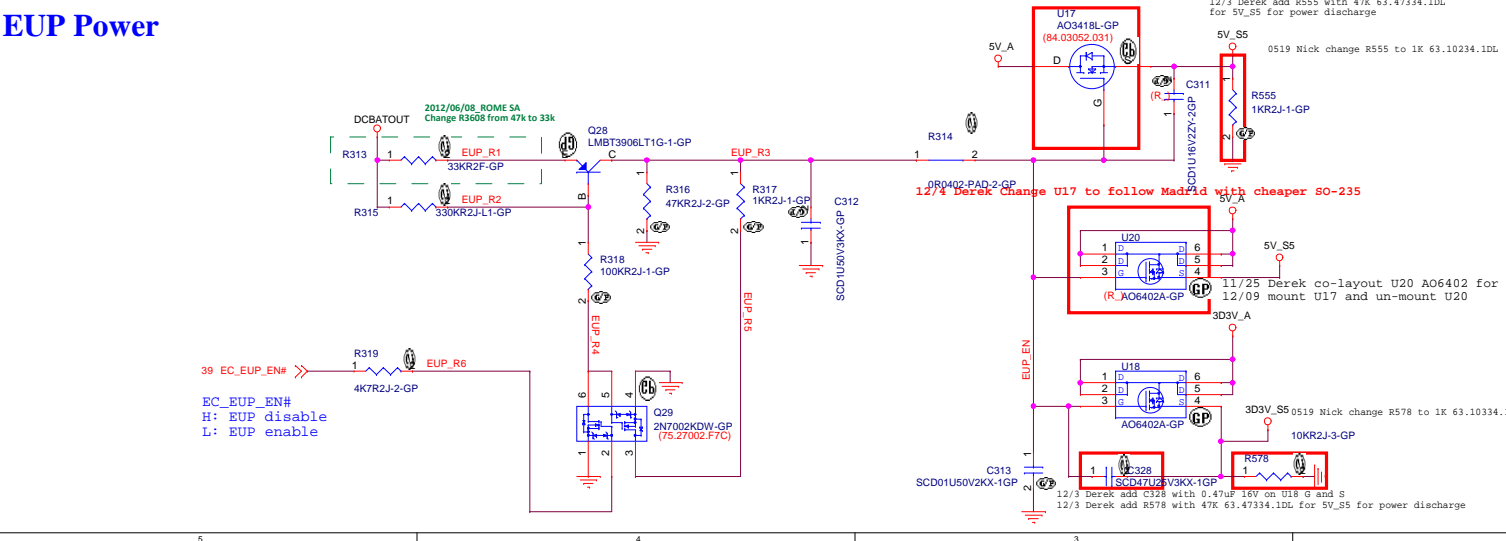
Rev
1A

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ANNIE Run Power



EUP Power



2012/10/19 David change from 84.04468.A37(11.6A) to 84.06402.B3D(7A)

2012/10/21 David Removed PS_S3CNTRL

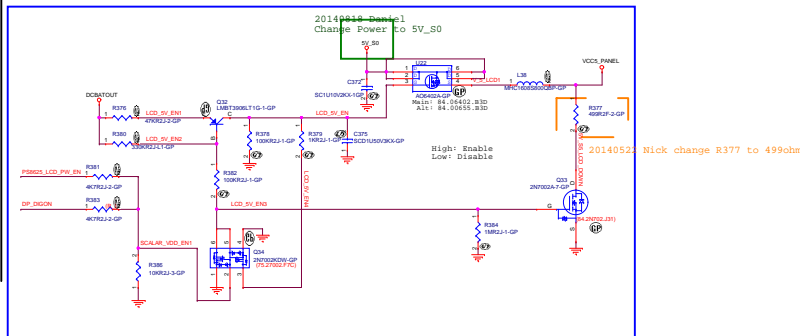
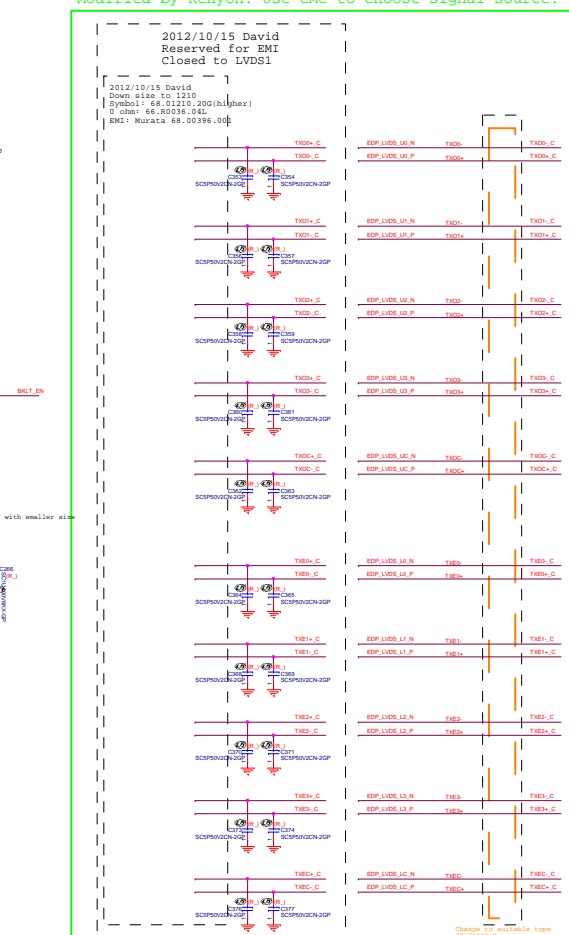
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Hsinchu, Taipei

File RUN POWER & SEQUENCE

Size Document Number Low Cost AIO

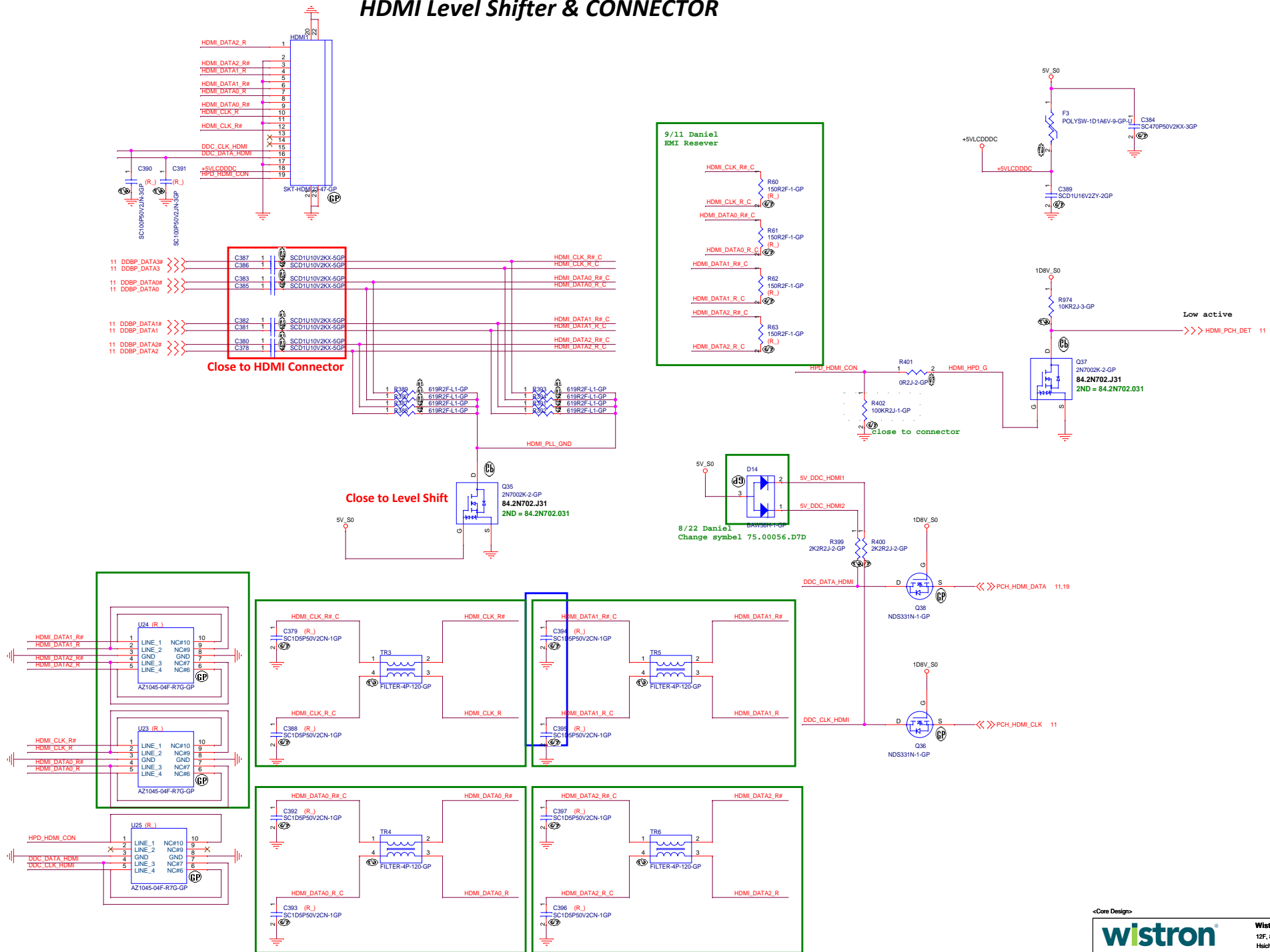
Date: Friday, September 12, 2014 Sheet 27 of 62

Modified by Kenyon. Use CMC to choose signal source. 2012/11/07



Panel Model	ID0	ID1	ID2	Vout
LG LM230WF3-SLK1	0	0	0	3.4 Vout 1.8 RTN 2.5V IN
LG LM230WF5-TLF1	0	0	1	3.4 Vout 1.8 RTN 2.5V IN
LG LM230WF5-SLL1	0	1	0	3.4 Vout 1.8 RTN 2.5V IN
CM1 M195FGE-L23 C1	1	0	0	1.2.5.6 Vout 3.4 RTN
CM1 M195FGE-L20 C3	1	1	0	1.2.5.6 Vout 3.4 RTN
CM1 M195FGE-L20 C1	1	1	1	1.2.5.6 Vout 3.4 RTN

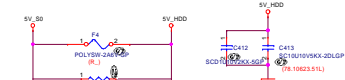
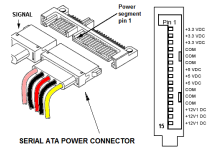
HDMI Level Shifter & CONNECTOR



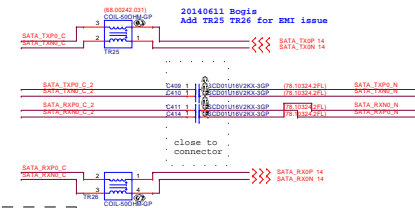
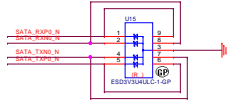
SSID = SATA

SATA HDD Connector

Layout: Put them together

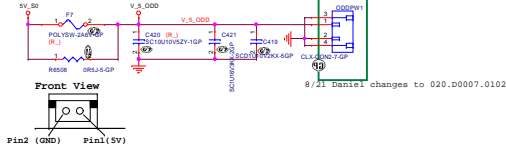
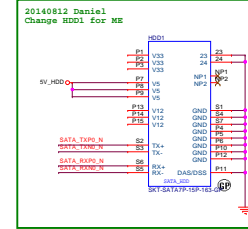


20140514 Nick add U15 TVS for RMI
20140516 Nick swap U15 net name



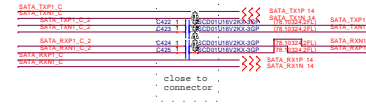
2012/10/5 David
Directly connected inside chip footprint for signal quality
(SA only!!!)

2012/10/10 David
SA create a temporary symbol (ZZ.08520.003) for re-driver co-lay,
if confirm that re-driver is required, need change symbol to
normal type (71.08520.003) , and cut short-pad inside the IC



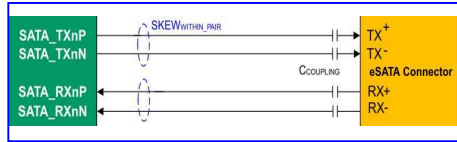
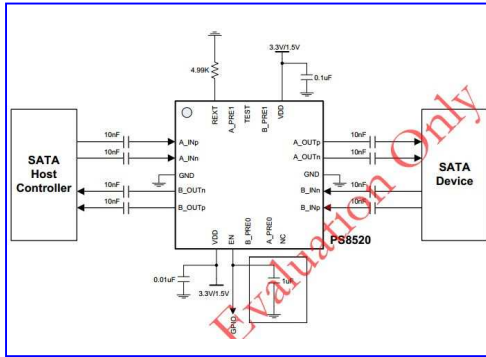
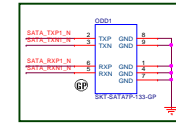
2012/10/23 David
change to PS8520 for SATA gen3

2013/05/21 David
Deleted SATA re-driver since
test PASS and to fix P/R issue



2012/10/24 David
EN pin and TEST pin can be floating for normal working.
Pin20 (REXT) should be connect to 4.99K ohm to GND

2012/10/10 David
SA create a temporary symbol (ZZ.08520.003) for re-driver co-lay,
if confirm that re-driver is required, need change symbol to
normal type (71.08520.003) , and cut short-pad inside the IC



VCC5_USB

DCBATOUT

1 R434 47KR2J-2-GP USB_EN1

1 R436 330KR2J-L1-GP USB_EN2

Q41 LMBT3906LT1G-1-GP

1 R435 47KR2J-2-GP

1 R437 1KR2J-1-GP

1 R438 100KR2J-1-GP

1 R439 4K7R2J-2-GP USB_EN6

Q42 2N7002KDW-GP (75.27002.F7C)

Q40 AO3418L-GP (84.03052.031) 3D3V_USB

USB_EN3

USB_EN4

USB_EN5

SLP_S5_N

USB_EN 34,36

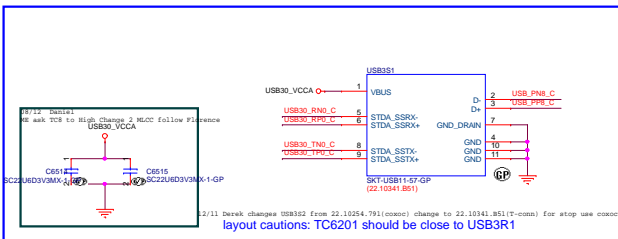
OR0402-PAD-2-GP



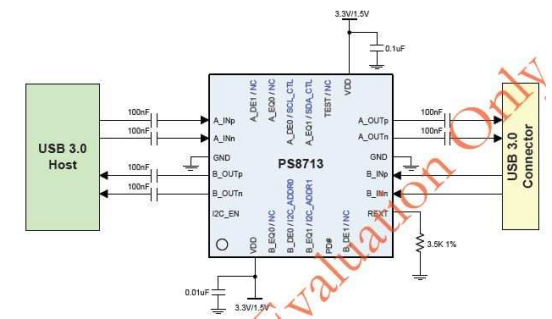
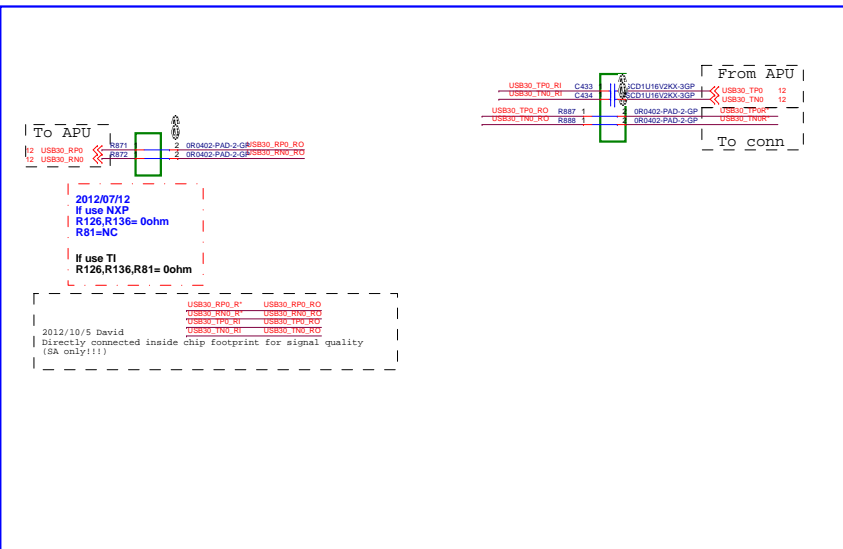
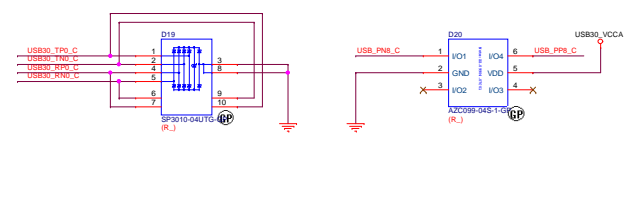
Title	USB 2.0 Power SW
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Rev	1A
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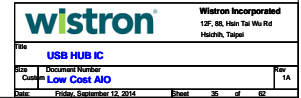
[illegible]

F_USBBP	F_USBBN
F_USBBP	F_USBBN



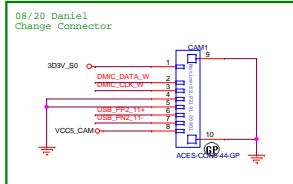
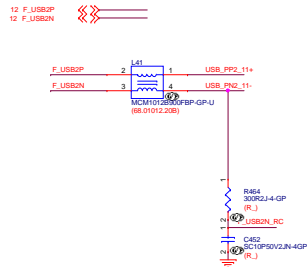
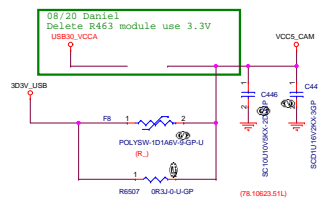
Enable/Disable USB output port: D+/D- pull high 1K to disable USB port
Set USB port to be internal (non-removable): set OC pin is floating
Set USB port to be external (removable): set OC pin is non-floating (pull high 10K to 3.3V or USB OC#)

Enable/Disable USB output port: setting by EEPROM
Set USB port to be internal (non-removable) or external (removable): setting by EEPROM

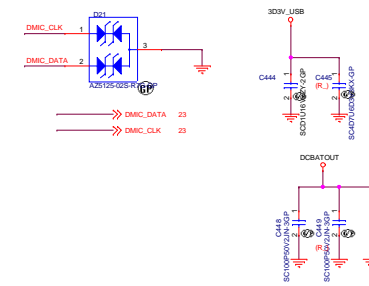


SSID =USB2.0

USB Port2 -> WEB CAM



DMIC Connector

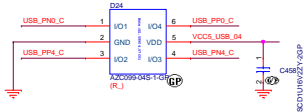
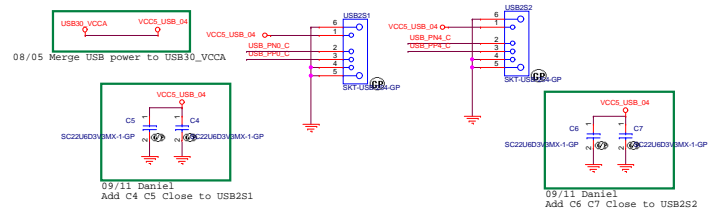


USB Port 1 -> Delete TOUCH

Mas touch Connector Pin Define	
PIN NO.	PIN Name
1	VUSB
2	D-
3	D+
4	GND
5	Shield

FK touch Connector Pin Define	
PIN NO.	PIN Name
1	VUSB
2	D-
3	D+
4	GND
5	Shield

USB Port -> Side I/O



SSID = Wireless and Bluetooth

Mini Card Connector(Wireless LAN+BT)

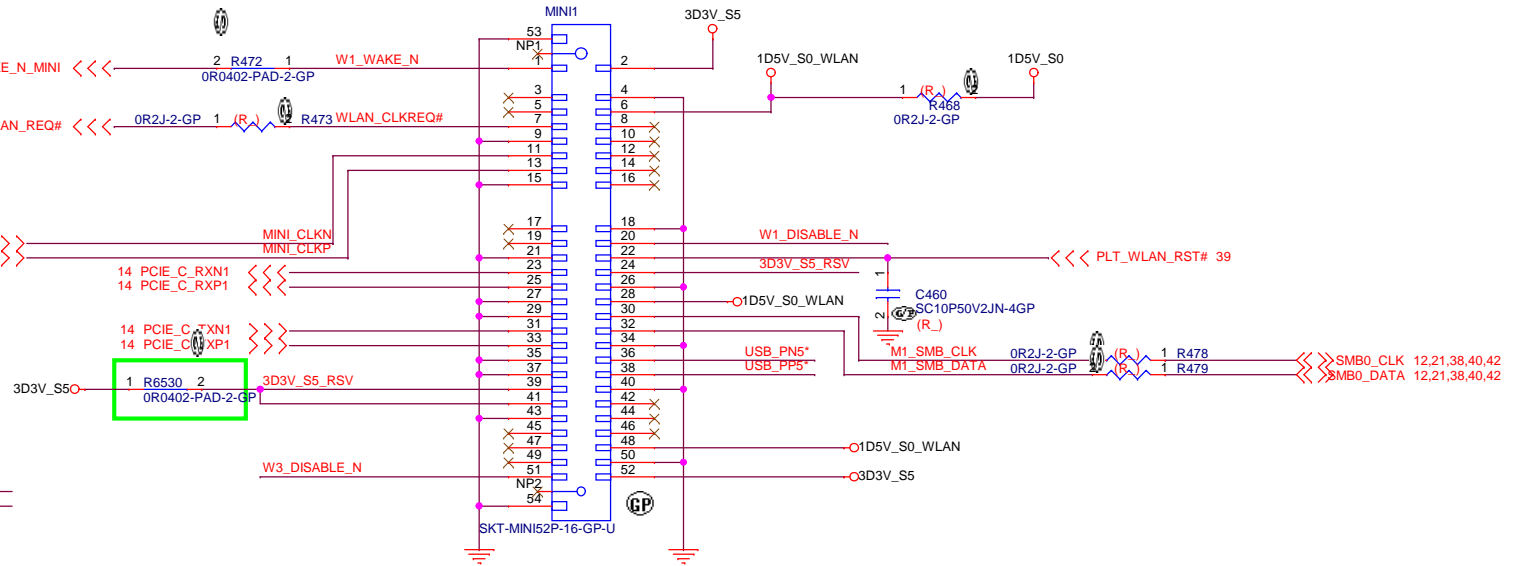
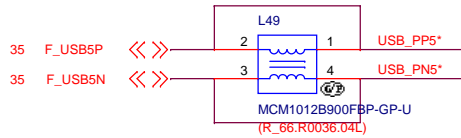
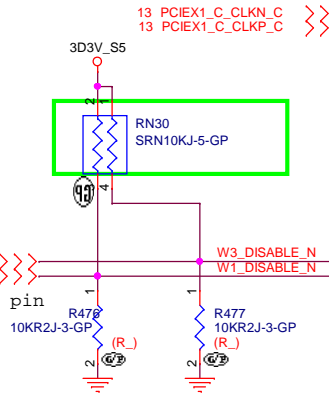
20140509 Nick R470
and R471 merge to
SRN0R

H: enable
L: disable

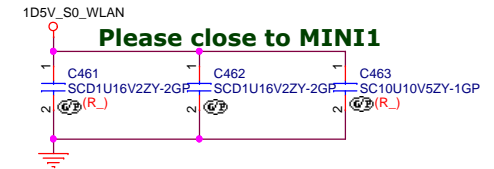
BT disable pin

39 W3_DISABLE_N
39 W1_DISABLE_N

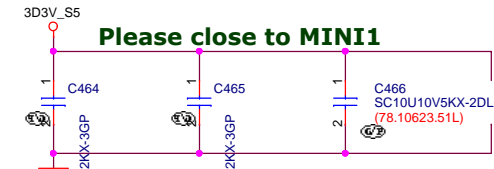
Wireless disable pin



Please close to MINI1



Please close to MINI1



<Variant Name>

wistron

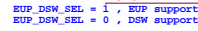
Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
MINI PCIE CARD (WLAN/BT)

Size
Document Number
Low Cost AIO

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1A

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USB Charger

5V Fan control

LCD ID

LPC

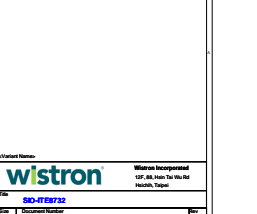
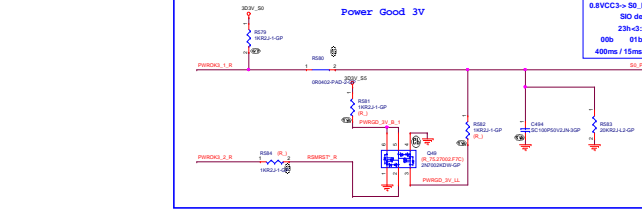
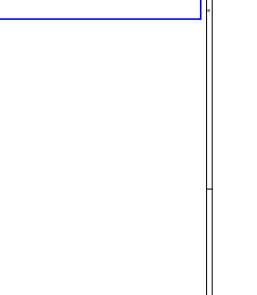
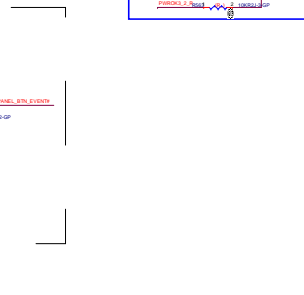
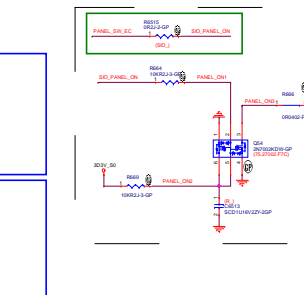
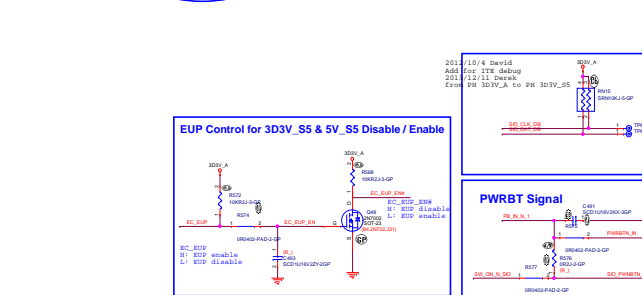
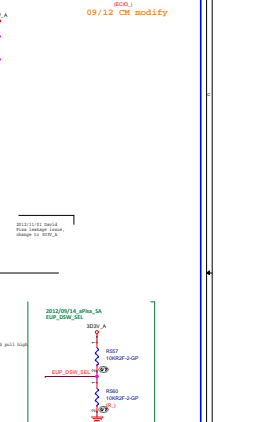
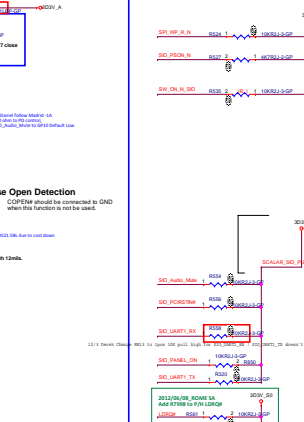
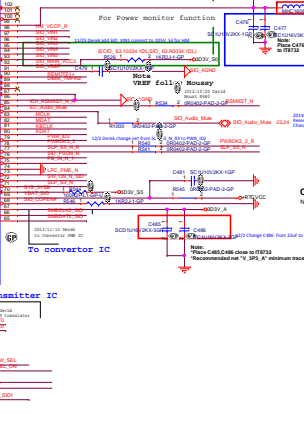
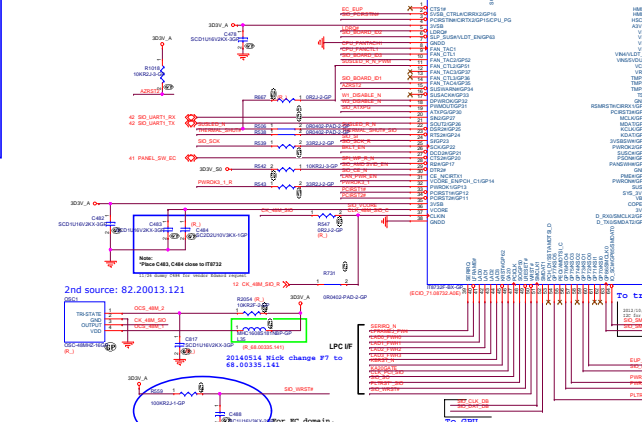
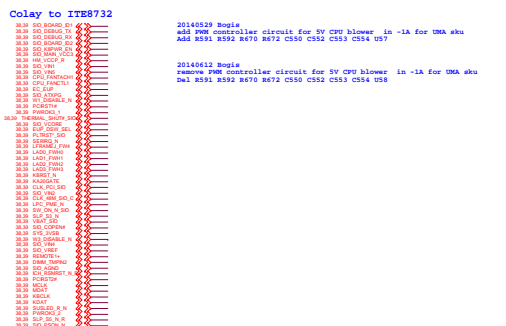
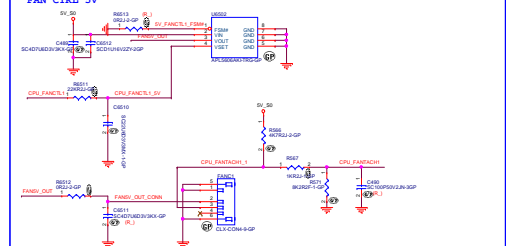
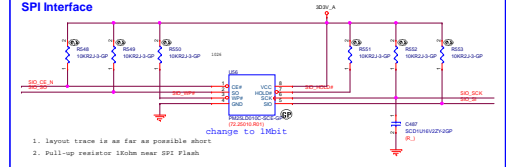
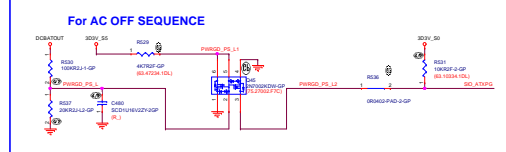
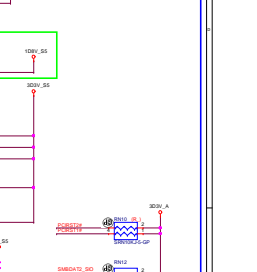
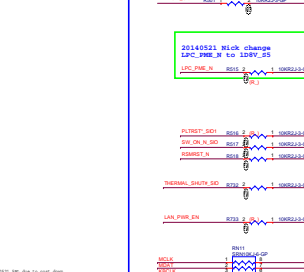
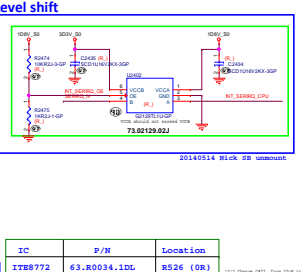
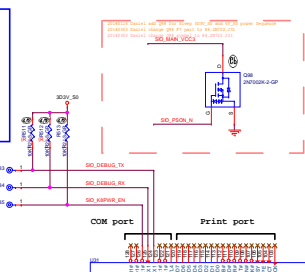
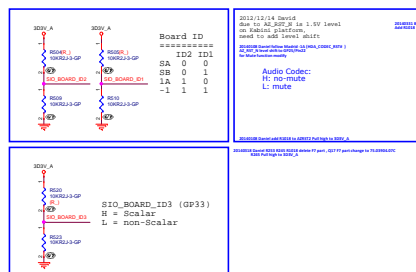
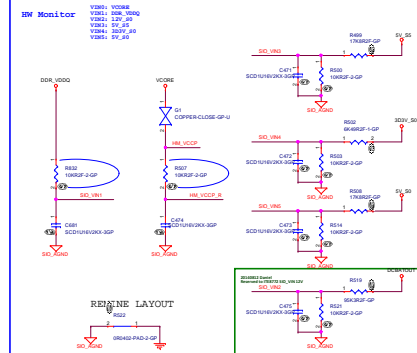
Power Manager

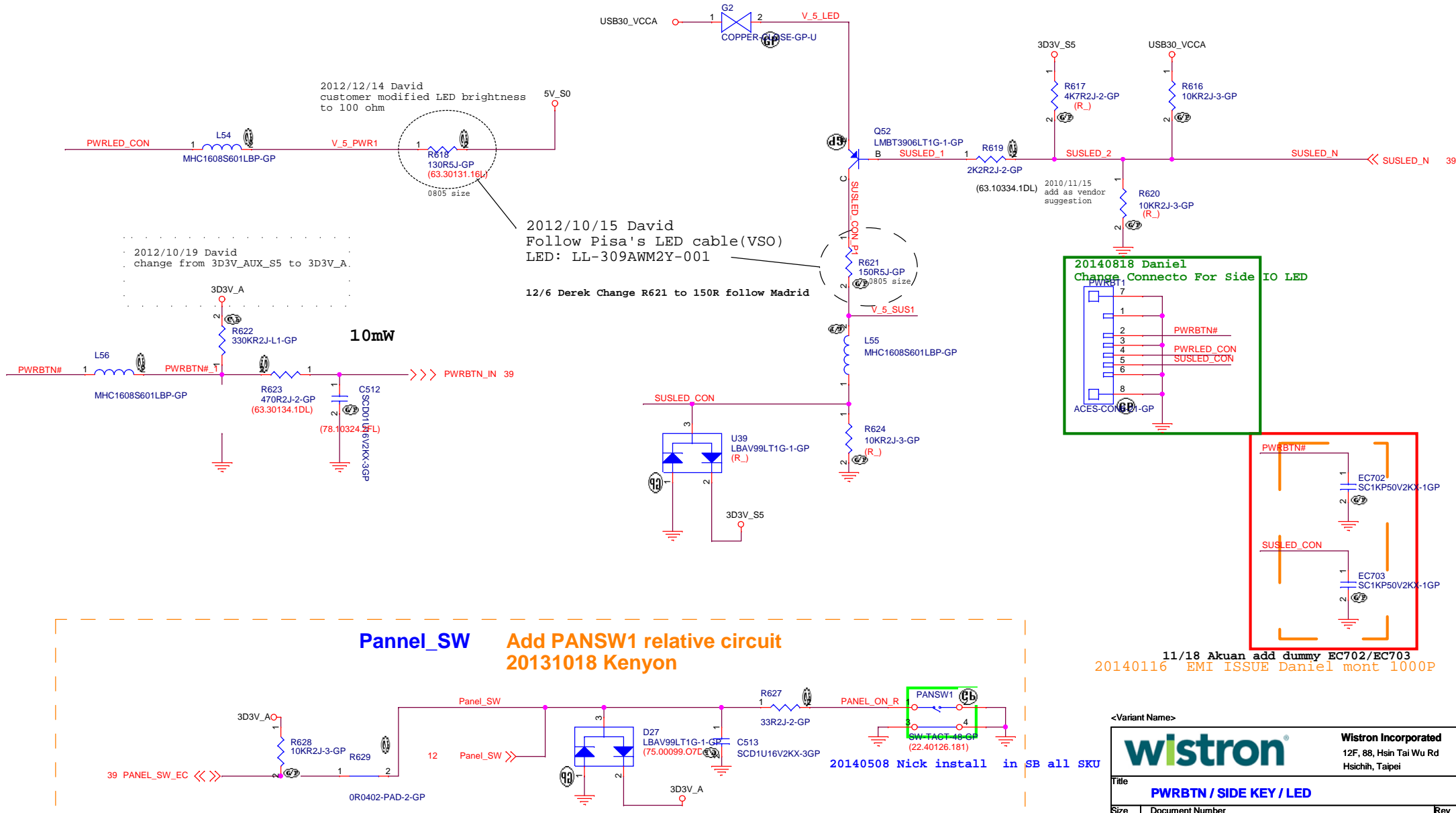
CLOCK


SMBUS

OTHERS

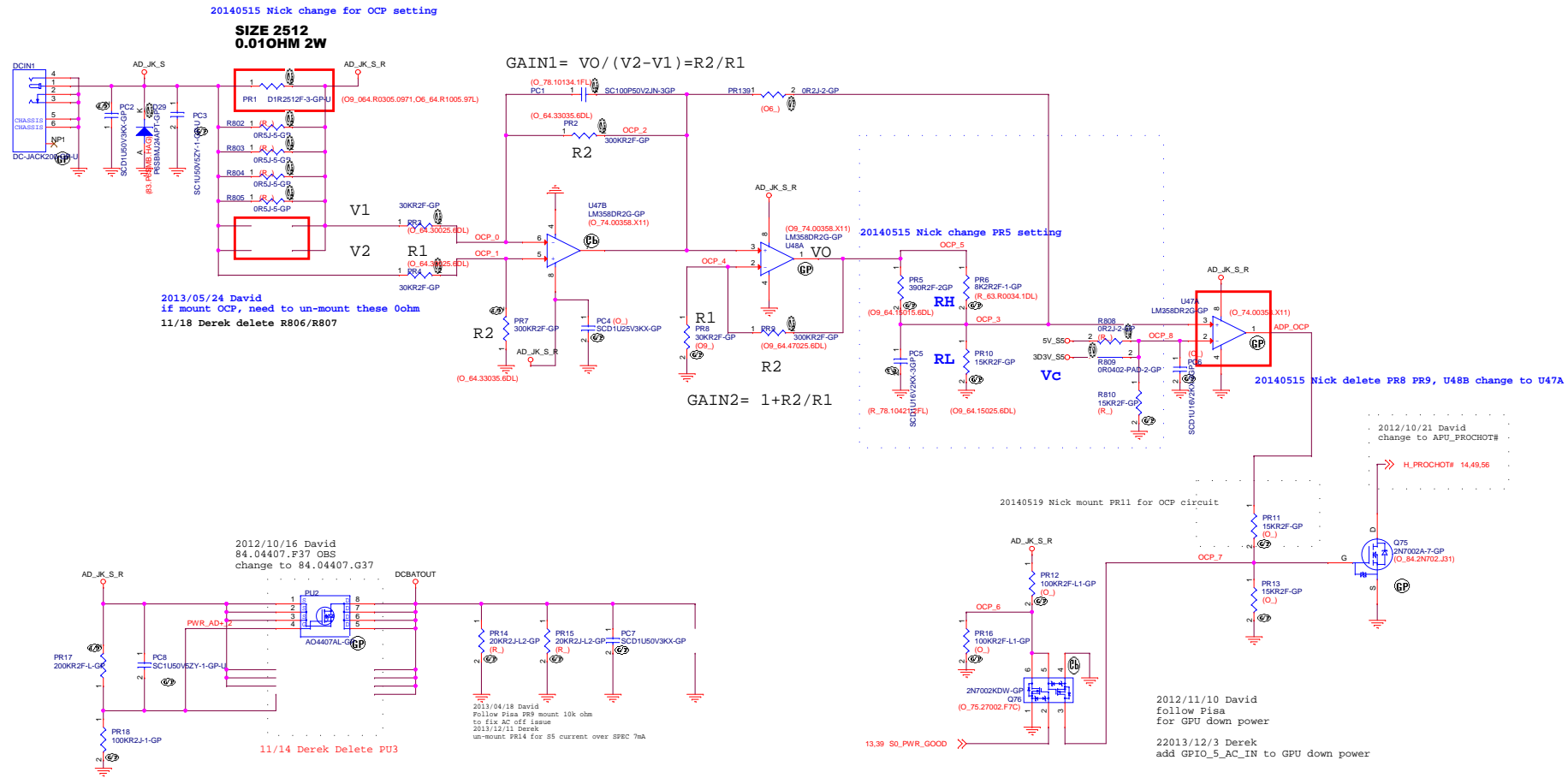
Panel On Off CTRL



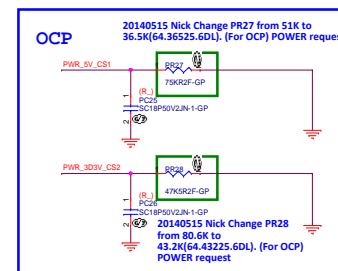
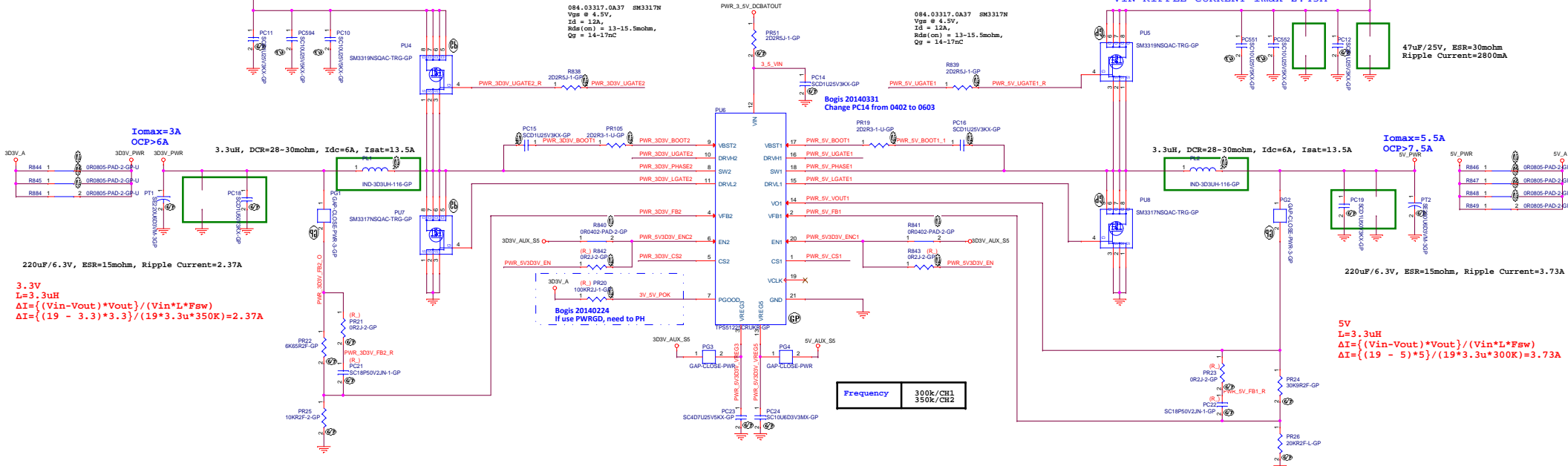
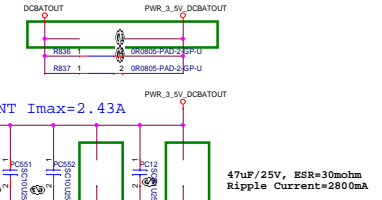
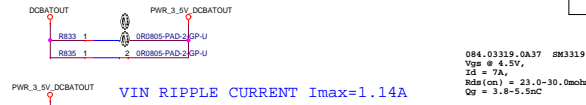


<Variant Name>		Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
			
Title PWRBTN / SIDE KEY / LED			
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ANNIE solution

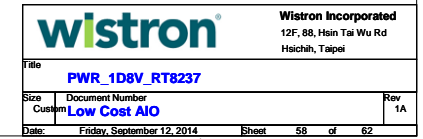


3D3V_PWR / 5V_PWR



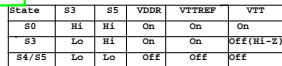
TONSEL	CH1	CH2	
GND	200kHz	250kHz	
VREF	300kHz	375kHz	
VREG3 or VREG5	400kHz	500kHz	

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto skip	Auto skip	PWM only



V_SM_VTT

EE need check


$$\Delta I = \frac{(V_{in} - V_{out}) \cdot V_{out}}{(V_{in} \cdot L \cdot F_{sw})}$$

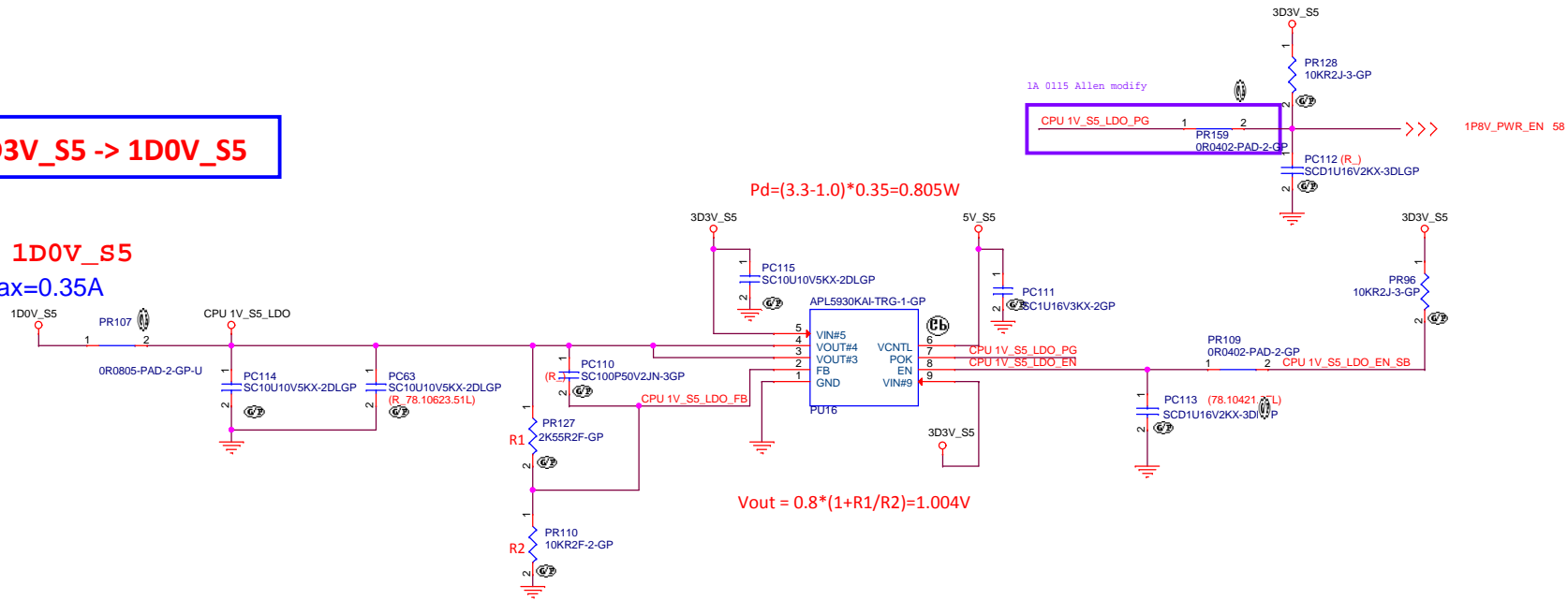
$$\Delta I = \frac{(19 - 1.35) \cdot 1.35}{(19 \cdot 0.82 \mu \cdot 800K)} = 1.91A$$

$$I_{\max} = 0.445A$$

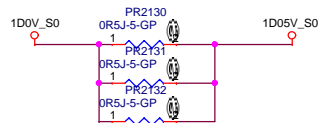
2014/4/28 Nick change from
1D05V_RUNPWROK to
+V_3P3_VGA

3D3V_S5 -> 1D0V_S5

CPU 1D0V_S5
I_{omax}=0.35A



Merger 1D05V_S0 -> 1D0V_S0



<Core Design>

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title
PWR_CPU 1V_S0&CPU 1V_S5

Size
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Material part

LGA115x CPU SOCKET Symbol

Vendor: LOTES
P/N: 22.78003.011

Vendor: FOXCONN
P/N: 22.78006.001

Vendor: LOTES
P/N: 22.78002.011
Thickness: max 2.2mm (含mylar及螺孔高)

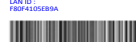
Vendor: FOXCONN
P/N: 22.78006.011
Thickness: 2.0mm (含mylar)

Vendor: LOTES
P/N: 22.78005.171

Vendor: FOXCONN
P/N: 22.78005.161

2013/03/19 David
Removed CPU socket & back plate & cover

LABEL



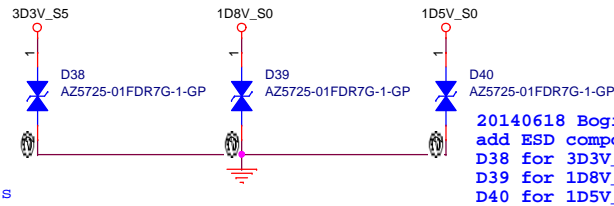
LBL1
LABEL
(40.3BZ24.001)

LBL2
LABEL
(R_)

LBL3
LABEL
(R_)

MB serial NO# and MAC address
40.3KP03.001 -> 35 x 15mm
45.41107.011 -> 70 x 8mm
45.41115.001 -> 34 x 13.5mm for aDallas
40.3BZ24.001 -> 30 x 15mm

09/24 Daniel
Change to 30x15 mm



Vendor: LOTES
P/N: 22.78005.171

Vendor: FOXCONN
P/N: 22.78005.161

20140618 Bogis
add ESD component
D38 for 3D3V_S5
D39 for 1D8V_S0
D40 for 1D5V_S0

HeatSink Symbol

2013/03/19 David
Removed HeatSink

Vendor
P/N:
60.3ET05.001
60.3ET05.011
60.3ET05.021

Battery Symbol



BTT2
BATTERY CR2032
(23.20068.001)

Vendor
P/N:
23.20068.001
23.20023.311
23.22063.001

Stand-off

2013/03/19 David
Removed Stand-off
since already exist

34.3KF01.001 for 5.2mm slot 62.10043.G11
34.3HJ03.001 for 9.0mm slot 62.10043.E41

PCB Symbol

<Core Design>

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Hsichih, Taipei

Title
HeatSink/Battery/etc

Size B Document Number
Low Cost AIO

Rev
1A

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TBD

GPI0	GP117
GPI00	FXL_PPMFIS_CLAMPDEBUS Sense
GPI01	MEM_VDD_CTL
GPI02	UNUSED
GPI03	UNUSED
GPI04	UNUSED
GPI05	Reserved
GPI06	FXL_CLAMP_TG1_REQ
GPI07	3DVision/UNUSED
GPI08	GPU Overtemp
GPI09	GPU Thermal Alert
GPI10	FB Hot Control
GPI11	NAVED PWRM_VSD
GPI12	PWR_Low AC Detect
GPI13	UNUSED (Reserved for future VSDs)
GPI14	N/A on Package
GPI15	N/A on Package
GPI16	N/A on Package
GPI17	N/A on Package
GPI18	N/A on Package
GPI19	N/A on Package
GPI20	N/A on Package
GPI21	N/A on Package

Table 115. GB2-64 and GB4-128 GPIO Description

Pin Name	Normal Function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	FB_CLAMP_A0H1	I	FB Clamp monitor	
GPIO1	MEM_VDD_CTL	O	Memory VDD VDD	MEM VDD: Strap to boot FBVDDQ
GPIO2	LC0_BL_PWM	O	Panel Backlight Pulse Brightness Control	100K pull-down
GPIO3	LC0_VCC	O	Panel Backlight Enable	LC0_VCC: 100K pull-down
GPIO4	LC0_BLDH	O	Panel Backlight Enable	100K pull-down
GPIO5	Reserved			
GPIO6	FXL_CLAMP_TG1_REQ	O	Active low FB Clamp toggle request	
GPIO7	3DVision	O	3D Vision L/R signal	100K pull-down
GPIO8	OVERT	I/O	Active Low Thermal Over Temperature	100K pull-up
GPIO9	ALERT	I/O	Active Low Thermal Alert	100K pull-up
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	PWRM_VSD	O	GPU Core VDD PwrM VSD signal	
GPIO12	PWRM_LEVEL	I	AC power plane power supply overdrive input	100K pull-up
GPIO13	PS	O	Power Switching	10K pull-up to enable two phase
GPIO14	HPD_A	I	Hot Plug Detect for HPD used as DisplayPort or for I2C when used as Dual Link DVI	See Figure 78
GPIO15	HPD_C	I	Hot Plug Detect for I2C	See Figure 78
GPIO16	FRM_LCK	I	21 Frame Lock signal	See Figure 78
GPIO17	HPD_B	I	Hot Plug Detect for I2C	See Figure 78
GPIO18	HPD_E	I	Hot Plug Detect for I2C	See Figure 78
GPIO19	HPD_F or HPD_B	I	Hot Plug Detect for I2C or for I2C used as DisplayPort	See Figure 78
GPIO20	Reserved			
GPIO21	Reserved			

• GPIO20 and GPIO21 are only available on H14M-GE/14M-GE/14M-HE/14M-H/14M-Q/14M-QV/14M-QV2
• The grouped section of Table 107 indicates GPIOs that are not available for H14M-Q/14M-QV2

GPIO0, GPIO6 is for G65 feature, no need to connect since this project won't support G65.
GPIO1 is for FB voltage control, no need to connect since the FBVDDQ is 1.5V for all P-States.
GPIO12: High-to-Ac Mode/Low-to-Battery Mode enter slow down function/pull for power saving/Recommend Pull-High for AC mode.
GPIO13 PBI: Change Phase from two to one, and then enter slow down function/pull for power saving.

Table 1. N14M-GE/GL DDR3 Recommended Memories 128Mx16 Configuration

Configuration	Vendor	Strap	FBVDDQ/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Data Code Minimum	Status
128Mx16 DDR3	Micron	0x1	1.5 V/ 1.5 V	MT41J128M16JT-09GK	1000	1150	Production Candidate
				MT41J128M16JT-107GK	900	1150	Production Candidate
	Samsung	0x5	1.5 V/ 1.5 V	K4V2G1646E-BC1A	1000	1204	Production Candidate
				K4V2G1646E-BC11	900	1204	Production Candidate
	Hynix	0x6	1.5V/ 1.5V	H5TQ2G63DFR-10C	1000	H/A	Production Candidate
				H5TQ2G63DFR-11C	900	H/A	Production Candidate

Table 2. N14M-GE/GL DDR3 Recommended Memories 256Mx16 Configuration

Configuration	Vendor	Strap	FBVDDQ/ FBVDDQ	Manufacturer Part Number	Max Speed CK (MHz)	Memory Data Code Minimum	Status
256Mx16 DDR3	Samsung	0x8	1.5 V/ 1.5 V	K4V4G1646B-HC11	900	H/A	Production Candidate
				HT41W256M16HA-107G-E	900	H/A	Production Candidate
	Micron	0x0	1.5 V/ 1.5 V	HT41W256M16HA-107G-E	900	H/A	Production Candidate
				H5TQ4G63AFR-11C	900	H/A	Production Candidate
	Hynix	0x3	1.5V/ 1.5V	H5TQ4G63AFR-11C	900	H/A	Production Candidate
				H5TQ4G63AFR-11C	900	H/A	Post-Production Candidate

Table 122 Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROH_SCLK	SUB_ALT_ADDR	10k Ω	Pull-down to GND
ROH_SI	SUB_VENOR	10k Ω	Pull-up to 3V3 if VBIOS ROM pin is pulled-down to GND if no VBIOS ROM
ROH_SO	VGA_DEVICE	10k Ω	Pull-down to GND (no display)
STRAP0	RAM_CFG[0]	10k Ω	See Note below
STRAP1	RAM_CFG[1]	10k Ω	See Note below
STRAP2	RAM_CFG[2]	10k Ω	See Note below
STRAP3	RAM_CFG[3]	10k Ω	See Note below
STRAP4	PCIE_MAX_SPEED	10k Ω	Pull-down to GND

Refer to the latest version of H14M-GE/GL Memory Recommended Vendor List for the specific setting for each memory type and configuration. Pull-up to 3V3 for binary '1' and pull-down to GND for binary '0'.

STRAP

STRAP PIN MODE TABLE	
PIN NAME	BINARY BRINGUP
STRAP0	3GIO_PADCFL_LUT_ADR0
STRAP1	3GIO_PADCFL_LUT_ADR1
STRAP2	3GIO_PADCFL_LUT_ADR2
STRAP3	3GIO_PADCFL_LUT_ADR3
STRAP4	PCI_MAX_SPEED
ROM_SCLK	SMU_ALT_ADDR
ROM_SI	SUB_VENOR
ROM_SO	VGA_DEVICE

NOTE 2: See table 1 for the correct recombination of the strap resistor for the desired mode.
NOTE 3: Bring-up SR030 have jumper configurable subvendor and DEVID_4 settings use the ROM_SCLK STRAP

XTAL

THERMAL PROTECTION

Mount	Un-mount	VRAM Type	P/N
R488 + R490 + R489 + R924	R483 + R486 + R929 + R934	Hynix 1Ghz H5TC2G63PFR-11C	KN.20B00.038
R483 + R490 + R929 + R934	R488 + R486 + R489 + R924	MICRON 1Ghz MT41J128M16JT-093GK	KN.20B04.022
R488 + R486 + R489 + R924	R483 + R490 + R929 + R934	SAMSUNG 1G K4W2G1646Q-BC1A	KN.20B0B.040

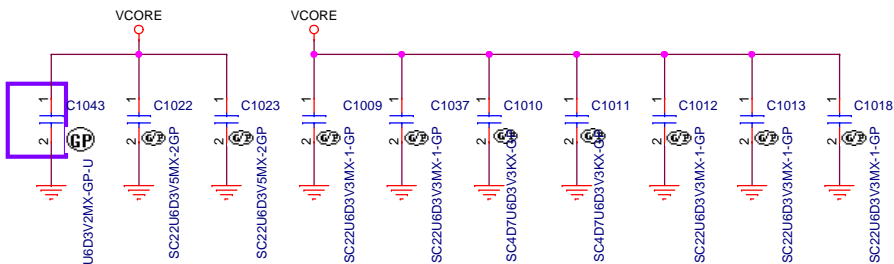
Mount 10K 64.10025.6DL

VRAM ID [0-3]:		VRAM ID [0-3]:			
VRAM Type	P/N	0	1	2	3
Hynix 1G H5TC2G63PFR-11C	KN.20B00.038	V	V	V	V
	72.52063.NOU	V	V	V	V

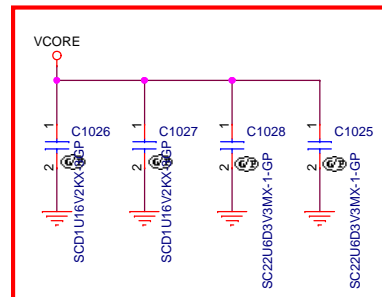
VRAM ID [0-3]:		VRAM ID [0-3]:			
VRAM Type	P/N	0	1	2	3
Micron 1G MT41J128M16JT-093GK	KN.20B04.022	V	V	V	V
	72.41128.TOU	V	V	V	V

VRAM ID [0-3]:		VRAM ID [0-3]:			
VRAM Type	P/N	0	1	2	3
SAMSUNG 1G K4W2G1646Q-BC1A	KN.20B0B.040	V	V	V	V
		V	V	V	V

VCORE

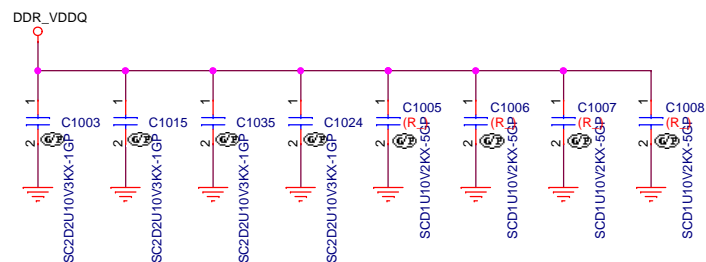


reserve the 0402 0.1u caps
on reset for EMI(5/9).

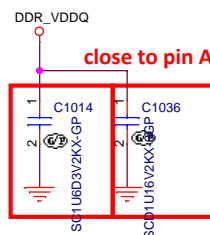


20150515 Nick add for power request

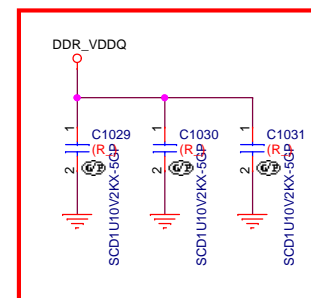
DDR_VDDQ



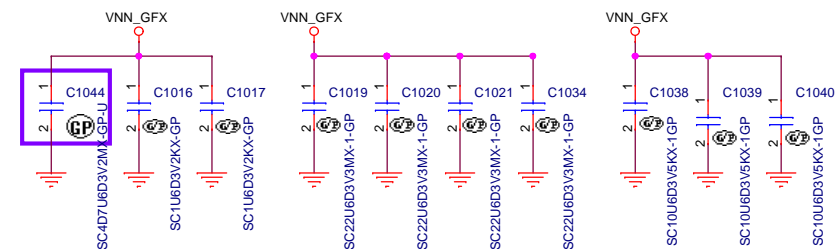
close to pin AD38 & AF38



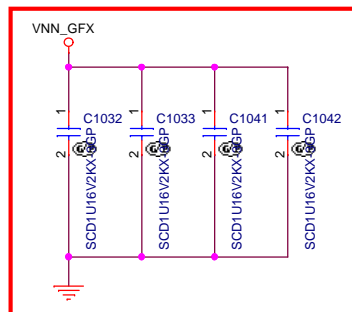
reserve the 0402 0.1u caps
on reset for EMI(5/9).



VNN_GFX



reserve the 0402 0.1u caps
on reset for EMI(5/9).



20150515 Nick add for power request

<Core Design>

wistron

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12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

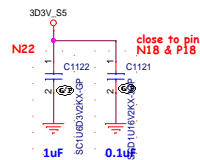
Title
CPU (POWER CAP1)

Size B Document Number
Low Cost A10

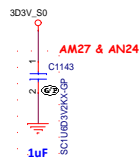
Rev
1A

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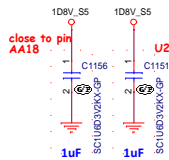
3D3V_S5



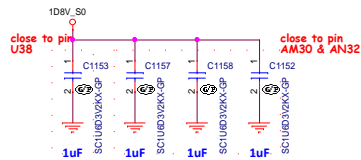
3D3V_S0



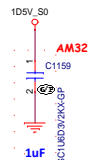
1D8V_S5



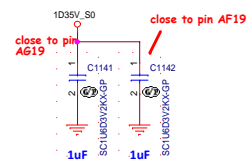
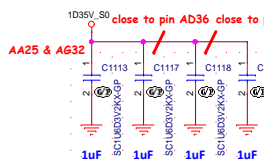
1D8V_S0



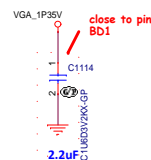
1D5V_S0



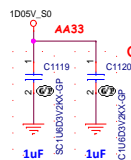
1D35V_S0



VGA_1P35V

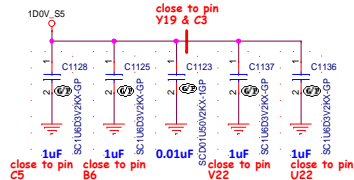


1D05V_S0

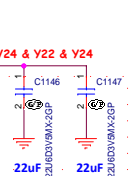
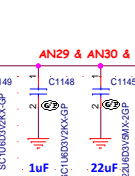
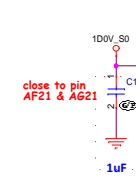
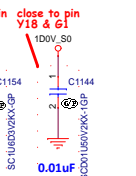
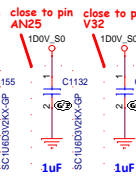
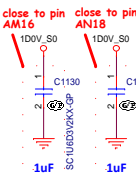
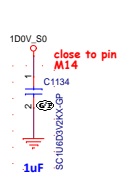
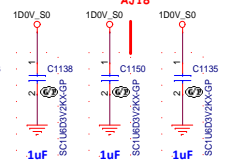
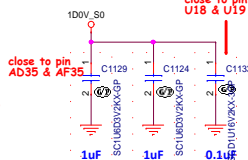
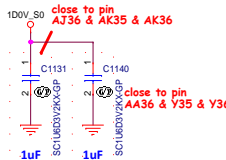
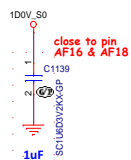


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1D0V_S5



1D0V_S0



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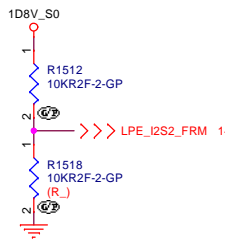
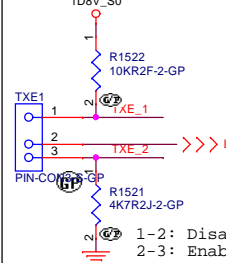
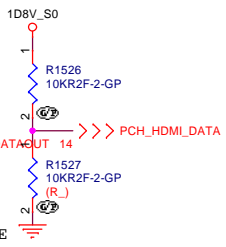
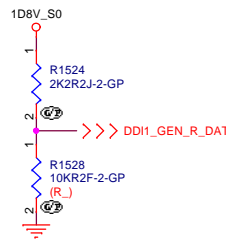
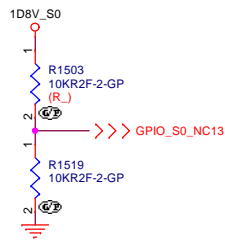
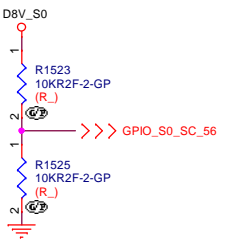
Size
Custom

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STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC
SHOULD BE PLACED OUTSIDE KOZ AREA

Description	BIOS Boot Selection	Security Flash Descriptors	DDI0 Detect	DDI1 Detect	DDI1 Detect	Top swap
GPIO	GPIO_S0_SC[063]	GPIO_S0_SC[065]	DDI0_DDCDATA	DDI1_DDCDATA	MDSI_DDCDATA	GPIO_S0_SC [56]
Schematic						
High	SPI	Normal Operation	DDI0 detected	DDI1 detected	DDI1 detected	
Low	LPC	Override	DDI0 not detected	DDI1 not detected	DDI1 not detected	

2.25 Hardware Straps

All straps are sampled on the rising edge of PMC_CORE_PWROK.

Table 27. Straps

Signal Name	Function	Default	Strap Exit	Strap Description
GPIO_S0_SC[63]	Legacy	1b	PMC_CORE_PWROK de-asserted	BIOS Boot Selection 0 = LPC 1 = SPI
GPIO_S0_SC[65]	Legacy	1b	PMC_CORE_PWROK de-asserted	Security Flash Descriptors 0 = Override 1 = Normal Operation
DDI0_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
DDI1_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected
MDSI_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected

27.1.1.2 Hardware Controlled

System hardware, external to the SoC, can be used to assert or de-assert the Top-Swap strapping input signal. If the signal is sampled as being asserted during power-up then Top-Swap is active.

Note: The Top-Swap strap is an active high signal and is multiplexed with the GPIO_S0_SC[56] signal.

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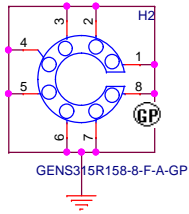
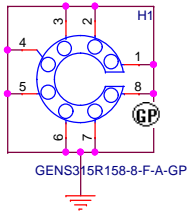
Size
A3

Document Number
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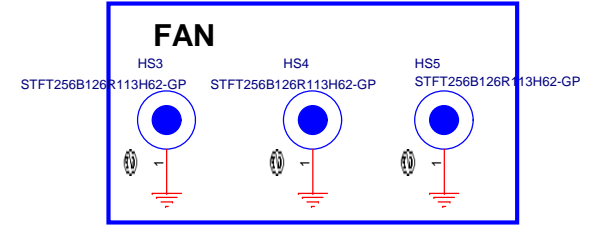
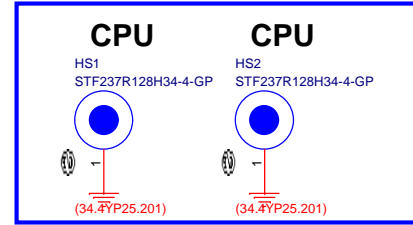
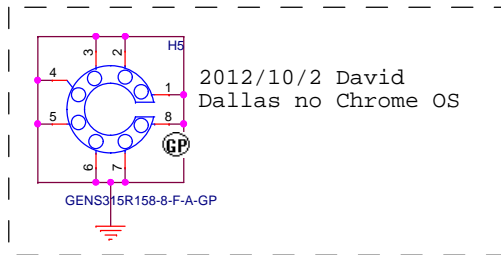
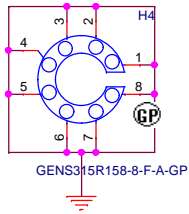
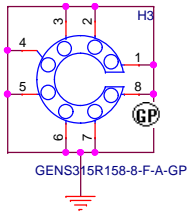
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